CONVEX

Field Support Tech Tip

Product: C-1
Tech Tip Number: CPU-001
Date: February 26, 1986
Subject: C-1 airflow sensors
Submitted By: Jim DeSmet

BACKGROUND

The aluminum colored air flow sensors (2 each) located in the main air duct at the back of the C-1 work on the principle that air can flow through the sensors. The sensors have two sets of holes, one facing the blower and one set toward the back of the C-1. If the air flow is blocked the system will shutdown with a temperature warning LED lit on the SMB. It is important to insure that the airflow holes are kept free of anything that might be blown in by the cooling fans.

The sensors work on the principle of a heating element inside the sensor trying to make two contacts come together. If the air flow is sufficient the temperature inside will not be high enough to allow the contact to close. Because of this another problem can be encountered if the heating element opens and no heat is generated. The sensor appears to work fine but would not protect the system in case of overheating. Therefore it is necessary to insure that the heater is working. To do this put an empty toilet tissue roll center over each sensor in turn to see that it does sense overtemperature and shutdown the system. The machine should power down within 30 seconds if the sensor works normally. If it does not power down the sensor is defective and should be replaced. It is recommended the machine be at the "(fp)>" prompt when these checks are made.

PROCEDURE

Quarterly

1. Vacuum the airflow sensors.
2. Insure each temperature sensor works by blocking the air flow and verifying the system recognizes the overtemperature condition. The SMB will illuminate an LED for each sensor as well as shutdown power within 30 seconds.

CONVEX

Field Support Tech Tip

Product: C-1
Tech Tip Number: CPU-002
Date: July 23, 1985 (Revised 3/1/87)
Subject: CPU Memory Boards
Submitted By: Dick Baker

Anytime additional memory is added to the C-1, diagnostic cpu4010 should be run. This diagnostic only tests the referenced and modified bits for existing memory. Should the referenced and modified bits for existing memory be bad, the file system could be corrupted.

When intermixing 4 MB, 16 MB, 32 MB, and/or 128 MB Memory Boards, the larger capacity boards must be in the lower-numbered MAU slots, the next larger in the next higher-numbered slots, etc.

CONVEX

Field Support Tech Tip

Product: C-1
Tech Tip Number: CPU-003
Date: December 19, 1987.
Subject: Airflow Sensor Board
Submitted By: Dick Baker

NOTE: This is a revision to the version of this Tech Tip dated July 2, 1983.

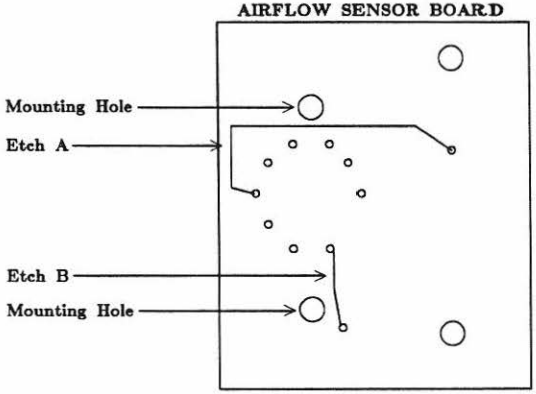
PROBLEM: During the evolution of the Airflow Sensor Board there have been a number of changes to the artwork. Some have been Convex initiated while others have been unauthorized vendor changes.

EFFECTIVITY: This Tech Tip addresses potential problems with the following items:

PART NUMBER	DESCRIPTION
411-000109-200	Airflow Sensor Assembly (Any Revision)
411-000109-500	Airflow Sensor FAB (Any Revision)

ACTION: When replacing the Airflow Sensor Assembly, **BEWARE** of clearance problems between the mounting holes and circuit traces (see **Etches** and **Holes** in illustration below). Some boards have no clearance problems, some require mounting screws with no flat washers, and some require an insulating washer to insulate the screw head from an etch. So, **BEWARE!** Failure to do so may result in a short circuit situation.

AIRFLOW SENSOR BOARD



CONVEX

Field Support Tech Tip

Product: C-1
Tech Tip Number: CPU-004
Date: December 15,1986
Subject: Power Cables
Submitted By: Dick Baker

NOTE: This is a revision to the version of this Tech Tip dated October 3, 1986.

There have been problems with the power cables from the power supply to the backplane dropping excessive (more than .15v) voltage due to improper crimping of the lug over the end of the braided cable. This problem is due to the vendor building the assembly incorrectly. The problem has been resolved with the supplier but there are defective units currently in customer machines.

This problem has the following symptoms:

1. Voltage difference greater than .15 volt between the voltage measured at the power supply terminals and the voltage measured between the ground bus at the bottom of the backplane and the top pin on the backplane.
2. Cable connector hot to the touch.
3. SPU senses voltage significantly lower than that measured at power supply.

A temporary solution is to more tightly crimp the lug with vise-grip pliers. The defective cable should still be replaced as soon as possible.

Part numbers for the cables are:

- 320-000135-500 +5 to IOP's (8 mounting screws) - 1 cable required
- 320-000135-501 +5 to JP/memory (10 mounting screws) - 2 cables required
- 320-000135-502 5 volt return for all 3 supplies

**** NOTE ****

- The power cables should be checked during **each and every** scheduled P.M. •

Field Support Tech Tip

Product: C-1
Tech Tip Number: CPU-005
Date: October 3, 1986
Subject: Voltage
Submitted By: Dick Baker

The +5 volt power supply voltage measurements should be taken using the ground bus at the bottom of the backplane as ground and the top pin of the appropriate backplane connector as the positive test point. Measuring at the power supply terminals or using the frame as ground can result in an error as great as .2 volts.

CONVEX

Field Support Tech Tip

Product: C-1
Tech Tip Number: CPU-006
Date: January 19, 1987
Subject: 128 MB Memory Addressing
Submitted By: Brad Jones

The intent of this Tech Tip is to describe the memory addressing scheme used in the C-1.

This Tech Tip is only valid for systems having a **maximum** memory capacity of 128 MB. 128 MB systems will utilize MCU Part Number 410-001123-200 **or** 410-002136-200. 1 GB (Cobra) systems utilize MCU Part Number 410-001136-200. The 1 GB memory addressing scheme is **not** discussed in this Tech Tip.

The C-1 Main Memory is initialized during '**initall**'. The format of the initialization message is shown below:

MAU	Allocated Blocks
A	BB BB ...BB
A	BB BB ...BB
.	
etc.	
.	
A	BB BB ...BB

WHERE: 'A' = An MAU number (any or all of **0** thru **7** possible).
'BB' = A series of 2-digit numbers, **each** of which represents a **2** MB block of memory on the MAU Board specified by the 'A' field. Functional **16** MB Boards will be shown as **00** thru **07**. Functional **4** MB boards will be shown as **00** AND **04**.

EXAMPLES:

•32 MB System (2 - 16MB Boards)

Main Memory Size: 33554432

MAU	Allocated Blocks
0	00 01 02 03 04 05 06 07
1	00 01 02 03 04 05 06 07
2	
3	
4	
5	
6	
7	

•Valid Memory Address Ranges

MAU	Address Ranges
0	00000000 thru 00FFFFFF
1	01000000 thru 01FFFFFF

•16 MB System (4 - 4 MB Boards)

Main Memory Size: 16777216

MAU	Allocated Blocks
0	00 04
1	00 04
2	00 04
3	00 04
4	
5	
6	
7	

•Valid Memory Address Ranges

MAU	Address Ranges
0	00000000 thru 001FFFFF
0	00800000 thru 009FFFFF
1	01000000 thru 011FFFFF
1	01800000 thru 019FFFFF
2	02000000 thru 021FFFFF
2	02800000 thru 029FFFFF
3	03000000 thru 031FFFFF
3	03800000 thru 039FFFFF

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The correlation of Memory Address-to-MAU Number and Allocated Blocks (see previous page) is shown in the following tables (**Note**: 'X' = don't care):

MAU			PHYSICAL (REAL) ADDRESS BITS																													
SIZE	ROW	BANK	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
16 MB	0	0	0	0	0	0	0				X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	X	X	X
	0	1	0	0	0	0	0				X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	X	X	X
	0	2	0	0	0	0	0				X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	X	X	X
	0	3	0	0	0	0	0	SEE			X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	X	X	X
	1	0	0	0	0	0	0	NOTE 1			X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	X	X	X
	1	1	0	0	0	0	0				X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	X	X	X
	1	2	0	0	0	0	0				X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	X	X	X
	1	3	0	0	0	0	0				X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	X	X	X
4 MB	0	0	0	0	0	0	0				0	0	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	X	X	X
	0	1	0	0	0	0	0				0	0	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	X	X	X
	0	2	0	0	0	0	0				0	0	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	X	X	X
	0	3	0	0	0	0	0	SEE			0	0	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	X	X	X
	1	0	0	0	0	0	0	NOTE 1			0	0	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	X	X	X
	1	1	0	0	0	0	0				0	0	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	X	X	X
	1	2	0	0	0	0	0				0	0	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	X	X	X
	1	3	0	0	0	0	0				0	0	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	X	X	X

NOTE 1 - The '**MAU**' (0-7) and '**Allocated Blocks**' (2 MB per Block) portions of the Memory Initialization Message (see previous page) are derived from the value of Memory Address Bits **26:23** as shown in the table below:

16 MB MAU						*	4 MB MAU					
ADDRESS BITS			MAU	ADDRESS	BLOCK	*	ADDRESS BITS			MAU	ADDRESS	BLOCK
26	25	24	NUMBER	BIT 23	NUMBER	*	26	25	24	NUMBER	BIT 23	NUMBER
0	0	0	0	0	00 - 03	*	0	0	0	0	0	00
0	0	1	1	1	04 - 07	*	0	0	1	1	1	04
0	1	0	2			*	0	1	0	2		
0	1	1	3			*	0	1	1	3		
1	0	0	4			*	1	0	0	4		
1	0	1	5			*	1	0	1	5		
1	1	0	6			*	1	1	0	6		
1	1	1	7			*	1	1	1	7		

As can be seen, the valid memory address range for 128 MB of memory space is (hexadecimal) **00000000** thru **07FFFFFF**.

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•Since MAU Read and Write accesses must be **longword**-oriented (8 bytes per longword), only a 24-bit memory address is required to access a full 128 MB of memory.

•A **physical** (real), 24-bit Memory Address is presented **to** the MCU **from** the IOP **or** the PCU. The evolution **from** a 32-bit **byte**-oriented address **to** a 24-bit **longword**-oriented address is illustrated below:

•32-BIT **PHYSICAL** ADDRESS
SENT **FROM** ATU **TO** PCU:

(SEE PAGE 4 FOR AN ILLUSTRATION OF **24-BIT** MEMORY ADDRESS FLOW THRU THE MCU, TO THE MAUs, AND WITHIN THE MAUs)

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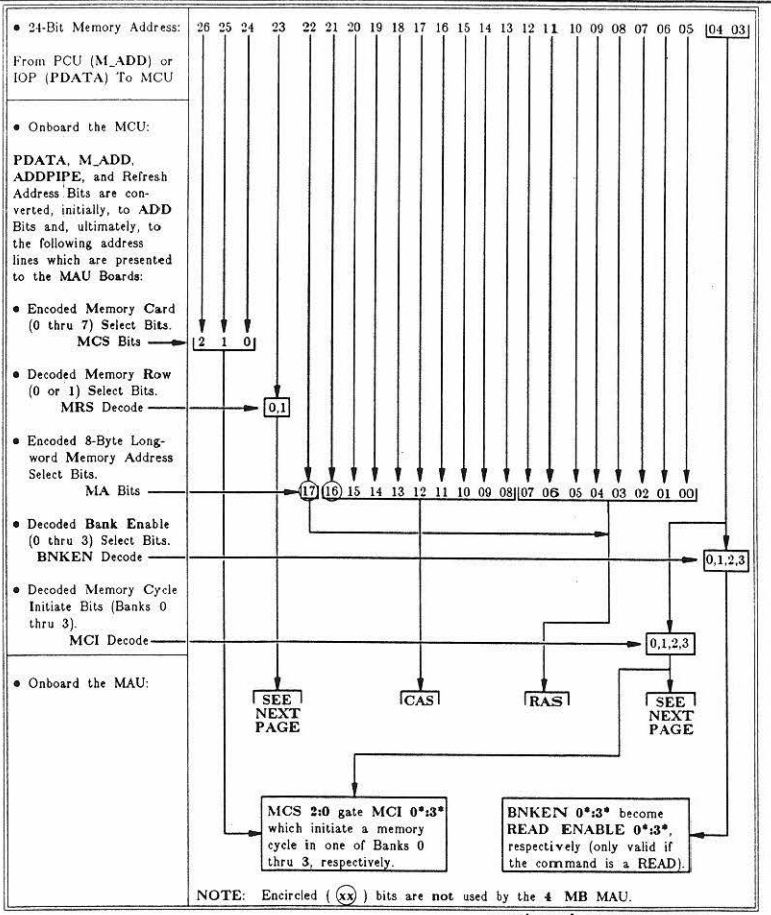

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- ONBOARD THE MCU -

- Memory Row Select Bit 0 (**MRS0***) becomes **B0ROWENAB0** thru **B3ROWENAB0**.
- Memory Row Select Bit 1 (**MRS1***) becomes **B0ROWENAB1** thru **B3ROWENAB1**.

These signals, in conjunction with **MCI 0*:3***, will select a group of RAMs as shown in the table below.

ACTIVE SIGNALS			DATA SELECTED		RAMS SELECTED		SELECTED	
CYCLE INITIATE	ROW SELECT	BANK/ROW ENABLE	BYTE NUMBERS	#BIT NUMBERS	*ODD BITS	*EVEN BITS	RAM BANK	RAM ROW
MCI0	MRS0	B0ROWENAB0	7:0	71:00	U125xy	U143xy	0	0
MCI0	MRS1	B0ROWENAB1	7:0	71:00	U116xy	U134xy	0	1
MCI1	MRS0	B1ROWENAB0	7:0	71:00	U089xy	U107xy	1	0
MCI1	MRS1	B1ROWENAB1	7:0	71:00	U080xy	U098xy	1	1
MCI2	MRS0	B2ROWENAB0	7:0	71:00	U053xy	U071xy	2	0
MCI2	MRS1	B2ROWENAB1	7:0	71:00	U044xy	U062xy	2	1
MCI3	MRS0	B3ROWENAB0	7:0	71:00	U017xy	U035xy	3	0
MCI3	MRS1	B3ROWENAB1	7:0	71:00	U008xy	U026xy	3	1

= Bits 71:64 are Check (**EDC**) Bits. Bits 63:00 are **DATA** Bits.

* = The value '**xy**' specifies the physical row and column coordinates of a RAM on the MAU board. The value of **x** can be a letter within the range **A** thru **T** and the value of **y** can be a number within the range **0** thru **9**. Reference the following pages for cross references of RAM locations to actual data bits.

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4 MB & 16 MB MAU RAM LOCATER TABLE

NOTE: Bit 00 (Byte 7) is **Least Significant**; Bit 63 (Byte 0) is **Most Significant**.

DATA			LOCATION					LOCATION			
BYTE	BIT	ROW	BANK 0	BANK 1	BANK 2	BANK 3	ROW	BANK 0	BANK 1	BANK 2	BANK 3
7	00	0	U143T1	U107T1	U071T1	U035T1	1	U134T1	U098T1	U062T1	U026T1
7	01	0	U125T1	U089T1	U053T1	U017T1	1	U116T1	U080T1	U044T1	U008T1
7	02	0	U143S7	U107S7	U071S7	U035S7	1	U134S7	U098S7	U062S7	U026S7
7	03	0	U125S7	U089S7	U053S7	U017S7	1	U116S7	U080S7	U044S7	U008S7
7	04	0	U143S3	U107S3	U071S3	U035S3	1	U134S3	U098S3	U062S3	U026S3
7	05	0	U125S3	U089S3	U053S3	U017S3	1	U116S3	U080S3	U044S3	U008S3
7	06	0	U143R9	U107R9	U071R9	U035R9	1	U134R9	U098R9	U062R9	U026R9
7	07	0	U125R9	U089R9	U053R9	U017R9	1	U116R9	U080R9	U044R9	U008R9
6	08	0	U143N9	U107N9	U071N9	U035N9	1	U134N9	U098N9	U062N9	U026N9
6	09	0	U125N9	U089N9	U053N9	U017N9	1	U116N9	U080N9	U044N9	U008N9
6	10	0	U143N5	U107N5	U071N5	U035N5	1	U134N5	U098N5	U062N5	U026N5
6	11	0	U125N5	U089N5	U053N5	U017N5	1	U116N5	U080N5	U044N5	U008N5
6	12	0	U143N1	U107N1	U071N1	U035N1	1	U134N1	U098N1	U062N1	U026N1
6	13	0	U125N1	U089N1	U053N1	U017N1	1	U116N1	U080N1	U044N1	U008N1
6	14	0	U143M7	U107M7	U071M7	U035M7	1	U134M7	U098M7	U062M7	U026M7
6	15	0	U125M7	U089M7	U053M7	U017M7	1	U116M7	U080M7	U044M7	U008M7
5	16	0	U143K7	U107K7	U071K7	U035K7	1	U134K7	U098K7	U062K7	U026K7
5	17	0	U125K7	U089K7	U053K7	U017K7	1	U116K7	U080K7	U044K7	U008K7
5	18	0	U143K3	U107K3	U071K3	U035K3	1	U134K3	U098K3	U062K3	U026K3
5	19	0	U125K3	U089K3	U053K3	U017K3	1	U116K3	U080K3	U044K3	U008K3
5	20	0	U143J9	U107J9	U071J9	U035J9	1	U134J9	U098J9	U062J9	U026J9
5	21	0	U125J9	U089J9	U053J9	U017J9	1	U116J9	U080J9	U044J9	U008J9
5	22	0	U143J5	U107J5	U071J5	U035J5	1	U134J5	U098J5	U062J5	U026J5
5	23	0	U125J5	U089J5	U053J5	U017J5	1	U116J5	U080J5	U044J5	U008J5
4	24	0	U143F2	U107F2	U071F2	U035F2	1	U134F2	U098F2	U062F2	U026F2
4	25	0	U125F2	U089F2	U053F2	U017F2	1	U116F2	U080F2	U044F2	U008F2
4	26	0	U143E8	U107E8	U071E8	U035E8	1	U134E8	U098E8	U062E8	U026E8
4	27	0	U125E8	U089E8	U053E8	U017E8	1	U116E8	U080E8	U044E8	U008E8
4	28	0	U143E4	U107E4	U071E4	U035E4	1	U134E4	U098E4	U062E4	U026E4
4	29	0	U125E4	U089E4	U053E4	U017E4	1	U116E4	U080E4	U044E4	U008E4
4	30	0	U143E0	U107E0	U071E0	U035E0	1	U134E0	U098E0	U062E0	U026E0
4	31	0	U125E0	U089E0	U053E0	U017E0	1	U116E0	U080E0	U044E0	U008E0
3	32	0	U143R5	U107R5	U071R5	U035R5	1	U134R5	U098R5	U062R5	U026R5
3	33	0	U125R5	U089R5	U053R5	U017R5	1	U116R5	U080R5	U044R5	U008R5
3	34	0	U143R1	U107R1	U071R1	U035R1	1	U134R1	U098R1	U062R1	U026R1
3	35	0	U125R1	U089R1	U053R1	U017R1	1	U116R1	U080R1	U044R1	U008R1

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4 MB & 16 MB MAU RAM LOCATER TABLE

NOTE: Bit 00 (Byte 7) is **Least Significant**; Bit 63 (Byte 0) is **Most Significant**.

DATA			LOCATION					LOCATION				
BYTE	BIT	ROW	BANK 0	BANK 1	BANK 2	BANK 3	ROW	BANK 0	BANK 1	BANK 2	BANK 3
3	36	0	U143P7	U107P7	U071P7	U035P7	1	U134P7	U098P7	U062P7	U026P7
3	37	0	U125P7	U089P7	U053P7	U017P7	1	U116P7	U080P7	U044P7	U008P7
3	38	0	U143P3	U107P3	U071P3	U035P3	1	U134P3	U098P3	U062P3	U026P3
3	39	0	U125P3	U089P3	U053P3	U017P3	1	U116P3	U080P3	U044P3	U008P3
2	40	0	U143M3	U107M3	U071M3	U035M3	1	U134M3	U098M3	U062M3	U026M3
2	41	0	U125M3	U089M3	U053M3	U017M3	1	U116M3	U080M3	U044M3	U008M3
2	42	0	U143L9	U107L9	U071L9	U035L9	1	U134L9	U098L9	U062L9	U026L9
2	43	0	U125L9	U089L9	U053L9	U017L9	1	U116L9	U080L9	U044L9	U008L9
2	44	0	U143L5	U107L5	U071L5	U035L5	1	U134L5	U098L5	U062L5	U026L5
2	45	0	U125L5	U089L5	U053L5	U017L5	1	U116L5	U080L5	U044L5	U008L5
2	46	0	U143L1	U107L1	U071L1	U035L1	1	U134L1	U098L1	U062L1	U026L1
2	47	0	U125L1	U089L1	U053L1	U017L1	1	U116L1	U080L1	U044L1	U008L1
1	48	0	U143J1	U107J1	U071J1	U035J1	1	U134J1	U098J1	U062J1	U026J1
1	49	0	U125J1	U089J1	U053J1	U017J1	1	U116J1	U080J1	U044J1	U008J1
1	50	0	U143H7	U107H7	U071H7	U035H7	1	U134H7	U098H7	U062H7	U026H7
1	51	0	U125H7	U089H7	U053H7	U017H7	1	U116H7	U080H7	U044H7	U008H7
1	52	0	U143H3	U107H3	U071H3	U035H3	1	U134H3	U098H3	U062H3	U026H3
1	53	0	U125H3	U089H3	U053H3	U017H3	1	U116H3	U080H3	U044H3	U008H3
1	54	0	U143F9	U107F9	U071F9	U035F9	1	U134F9	U098F9	U062F9	U026F9
1	55	0	U125F9	U089F9	U053F9	U017F9	1	U116F9	U080F9	U044F9	U008F9
0	56	0	U143D6	U107D6	U071D6	U035D6	1	U134D6	U098D6	U062D6	U026D6
0	57	0	U125D6	U089D6	U053D6	U017D6	1	U116D6	U080D6	U044D6	U008D6
0	58	0	U143D2	U107D2	U071D2	U035D2	1	U134D2	U098D2	U062D2	U026D2
0	59	0	U125D2	U089D2	U053D2	U017D2	1	U116D2	U080D2	U044D2	U008D2
0	60	0	U143C8	U107C8	U071C8	U035C8	1	U134C8	U098C8	U062C8	U026C8
0	61	0	U125C8	U089C8	U053C8	U017C8	1	U116C8	U080C8	U044C8	U008C8
0	62	0	U143C4	U107C4	U071C4	U035C4	1	U134C4	U098C4	U062C4	U026C4
0	63	0	U125C4	U089C4	U053C4	U017C4	1	U116C4	U080C4	U044C4	U008C4
EDC	64	0	U143C0	U107C0	U071C0	U035C0	1	U134C0	U098C0	U062C0	U026C0
EDC	65	0	U125C0	U089C0	U053C0	U017C0	1	U116C0	U080C0	U044C0	U008C0
EDC	66	0	U143B6	U107B6	U071B6	U035B6	1	U134B6	U098B6	U062B6	U026B6
EDC	67	0	U125B6	U089B6	U053B6	U017B6	1	U116B6	U080B6	U044B6	U008B6
EDC	68	0	U143B2	U107B2	U071B2	U035B2	1	U134B2	U098B2	U062B2	U026B2
EDC	69	0	U125B2	U089B2	U053B2	U017B2	1	U116B2	U080B2	U044B2	U008B2
EDC	70	0	U143A8	U107A8	U071A8	U035A8	1	U134A8	U098A8	U062A8	U026A8
EDC	71	0	U125A8	U089A8	U053A8	U017A8	1	U116A8	U080A8	U044A8	U008A8

...continued on next page

4 MB & MB MAU RAM LAYOUT

BANK 3				BANK 2				BANK 1				BANK 0				
ROW1	ROW0	ROW1	ROW0	ROW1	ROW0	ROW1	ROW0	ROW1	ROW0	ROW1	ROW0	ROW1	ROW0	ROW1	ROW0	
U008	U017	U026	U035	U044	U053	U062	U071	U080	U089	U098	U107	U116	U125	U134	U143	
D01	D01	D00	D00	D01	D01	D00	D00	D01	D01	D00	D00	D01	D01	D00	D00	T1
D03	D03	D02	D02	D03	D03	D02	D02	D03	D03	D02	D02	D03	D03	D02	D02	S7
D05	D05	D04	D04	D05	D05	D04	D04	D05	D05	D04	D04	D05	D05	D04	D04	S3
D07	D07	D06	D06	D07	D07	D06	D06	D07	D07	D06	D06	D07	D07	D06	D06	R9
D83	D83	D82	D82	D83	D83	D82	D82	D83	D83	D82	D82	D83	D83	D82	D82	R5
D85	D85	D84	D84	D85	D85	D84	D84	D85	D85	D84	D84	D85	D85	D84	D84	R1
D87	D87	D86	D86	D87	D87	D86	D86	D87	D87	D86	D86	D87	D87	D86	D86	P7
D89	D89	D88	D88	D89	D89	D88	D88	D89	D89	D88	D88	D89	D89	D88	D88	P3
D09	D09	D08	D08	D09	D09	D08	D08	D09	D09	D08	D08	D09	D09	D08	D08	N9
D11	D11	D10	D10	D11	D11	D10	D10	D11	D11	D10	D10	D11	D11	D10	D10	N5
D13	D13	D12	D12	D13	D13	D12	D12	D13	D13	D12	D12	D13	D13	D12	D12	N1
D15	D15	D14	D14	D15	D15	D14	D14	D15	D15	D14	D14	D15	D15	D14	D14	M7
D41	D41	D40	D40	D41	D41	D40	D40	D41	D41	D40	D40	D41	D41	D40	D40	M3
D43	D43	D42	D42	D43	D43	D42	D42	D43	D43	D42	D42	D43	D43	D42	D42	L9
D45	D45	D44	D44	D45	D45	D44	D44	D45	D45	D44	D44	D45	D45	D44	D44	L5
D47	D47	D46	D46	D47	D47	D46	D46	D47	D47	D46	D46	D47	D47	D46	D46	L1
D17	D17	D16	D16	D17	D17	D16	D16	D17	D17	D16	D16	D17	D17	D16	D16	K7
D19	D19	D18	D18	D19	D19	D18	D18	D19	D19	D18	D18	D19	D19	D18	D18	K3
D21	D21	D20	D20	D21	D21	D20	D20	D21	D21	D20	D20	D21	D21	D20	D20	J9
D23	D23	D22	D22	D23	D23	D22	D22	D23	D23	D22	D22	D23	D23	D22	D22	J5
D49	D49	D48	D48	D49	D49	D48	D48	D49	D49	D48	D48	D49	D49	D48	D48	J1
D61	D61	D60	D60	D61	D61	D60	D60	D61	D61	D60	D60	D61	D61	D60	D60	H7
D63	D63	D62	D62	D63	D63	D62	D62	D63	D63	D62	D62	D63	D63	D62	D62	H3
D65	D65	D64	D64	D65	D65	D64	D64	D65	D65	D64	D64	D65	D65	D64	D64	F9
D25	D25	D24	D24	D25	D25	D24	D24	D25	D25	D24	D24	D25	D25	D24	D24	F5
D27	D27	D26	D26	D27	D27	D26	D26	D27	D27	D26	D26	D27	D27	D26	D26	E8
D29	D29	D28	D28	D29	D29	D28	D28	D29	D29	D28	D28	D29	D29	D28	D28	E4
D81	D81	D80	D80	D81	D81	D80	D80	D81	D81	D80	D80	D81	D81	D80	D80	E0
D67	D67	D66	D66	D67	D67	D66	D66	D67	D67	D66	D66	D67	D67	D66	D66	D6
D69	D69	D68	D68	D69	D69	D68	D68	D69	D69	D68	D68	D69	D69	D68	D68	D2
D01	D01	D00	D00	D01	D01	D00	D00	D01	D01	D00	D00	D01	D01	D00	D00	C8
D03	D03	D02	D02	D03	D03	D02	D02	D03	D03	D02	D02	D03	D03	D02	D02	C4
EDC85	EDC85	EDC84	EDC84	EDC85	EDC85	EDC84	EDC84	EDC85	EDC85	EDC84	EDC84	EDC85	EDC85	EDC84	EDC84	C0
EDC87	EDC87	EDC86	EDC86	EDC87	EDC87	EDC86	EDC86	EDC87	EDC87	EDC86	EDC86	EDC87	EDC87	EDC86	EDC86	B6
EDC89	EDC89	EDC88	EDC88	EDC89	EDC89	EDC88	EDC88	EDC89	EDC89	EDC88	EDC88	EDC89	EDC89	EDC88	EDC88	B2
EDC71	EDC71	EDC70	EDC70	EDC71	EDC71	EDC70	EDC70	EDC71	EDC71	EDC70	EDC70	EDC71	EDC71	EDC70	EDC70	A8

CONVEX

Field Support Tech Tip

Product: C-1, JUNIOR, & OREO
Tech Tip Number: CPU-007
Date: January 20, 1987 (Rev. 4/15/87)
Subject: CPU Class & Serial Number
Submitted By: Brad Jones

The CPU *Serial Number* and, if applicable, *Class* are determined by Backplane strapping. Depending on the version of System Diagnostics **and** the revision level of the SPU Board (410-001131-200), the Serial Number and, possibly, the Class information can be seen at the Front Panel Menu (derived from SPU Board) **and** in the 'cop' information (derived from System Diagnostics).

As of this date, possible *classes* are: **0** (C-1; Standard or Rattlesnake)
1 (Junior only)
2 (Oreo only)

The tables below show the information that will be seen depending upon the possible combinations of System Diagnostics and SPU Revision levels.

- **Example 1** - Junior System (Class **1**) with Serial Number **200**.

REVISION LEVELS		INFORMATION DISPLAYED			
SPU BOARD	SYSTEM DIAGNOSTICS	AT THE FRONT PANEL [(fp)>] MENU		AS A RESULT OF THE 'cop' COMMAND	
		CLASS	S/N	CLASS	S/N
E and Earlier	4.1 and Earlier	NONE	4296	NONE	4296
F only	5.0 and 6.0	1	200	1	200
G and Later	6.1 and Later	1	4296	1	4296

- **Example 2** - Standard C-1 (Class **0**) with Serial Number **200**.

REVISION LEVELS		INFORMATION DISPLAYED			
SPU BOARD	SYSTEM DIAGNOSTICS	AT THE FRONT PANEL [(fp)>] MENU		AS A RESULT OF THE 'cop' COMMAND	
		CLASS	S/N	CLASS	S/N
E and Earlier	4.1 and Earlier	NONE	200	NONE	200
F and Later	5.0 and Later	0	200	0	200

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Serial Number **and** *Class* identification are strapped at the **SPU** Slot, Connector **P2**, Pins **B01** *thru* **B16**. An **open** pin will equal a '**1**' and a pin wired to a corresponding pin in Row **Y** (**e.g., Y01** *thru* **Y16**) will equal a '**0**'. Pins **B01** *thru* **B04** identify the **Class** and pins **B05** *thru* **B16** are for **Serial Number** Identification.

- The example below shows strapping to identify a Junior System (Class **1**) with Serial Number **150**. Note that, depending on the SPU Board Revision Level **and** the Version of System Diagnostics, the **Class** can be reported as **1** *or* not at all and the Serial Number can be reported as **150** (Binary 128 + 16 + 4 + 2) *or* as **4246** (Binary 4096 + 128 + 16 + 4 + 2). Reference previous page for other examples.

SPU SLOT - CONNECTOR P2	Y C B A	BINARY WEIGHT	USAGE
01	• • • •	8 *and/or* 32768	Class
02	• • • •	4 *and/or* 16384	Class
03	• • • •	2 *and/or* 8192	Class
04	• • • •	1 *and/or* 4096	Class
05	• • • •	2048 (Most Significant)	Serial Number
06	• • • •	1024	Serial Number
07	• • • •	512	Serial Number
08	• • • •	256	Serial Number
09	• • • •	128	Serial Number
10	• • • •	64	Serial Number
11	• • • •	32	Serial Number
12	• • • •	16	Serial Number
13	• • • •	8	Serial Number
14	• • • •	4	Serial Number
15	• • • •	2	Serial Number
16	• • • •	1 (Least Significant)	Serial Number
17	• • • •		No Connection
**	•		*
**	•		*
32	• • • •		No Connection

EXAMPLE

The following strapping is required for a Junior System (*Class* **1**) that is to have *Serial Number* **150**.

- **Class 1 Strapping:**
  - **B01 to Y01**
  - **B02 to Y02**
  - **B03 to Y03**
  - **B04 OPEN**
- **Serial Number 150 Strapping:**
  - **B05 to Y05**
  - **B06 to Y06**
  - **B07 to Y07**
  - **B08 to Y08**
  - **B09 OPEN**
  - **B10 to Y10**
  - **B11 to Y11**
  - **B12 OPEN**
  - **B13 to Y13**
  - **B14 OPEN**
  - **B15 OPEN**
  - **B16 to Y16**

To summarize, those systems that have a Revision G or later SPU **Board and** Version 6.1 or later System Diagnostics will be identifiable by Serial Number *range* as is shown below.

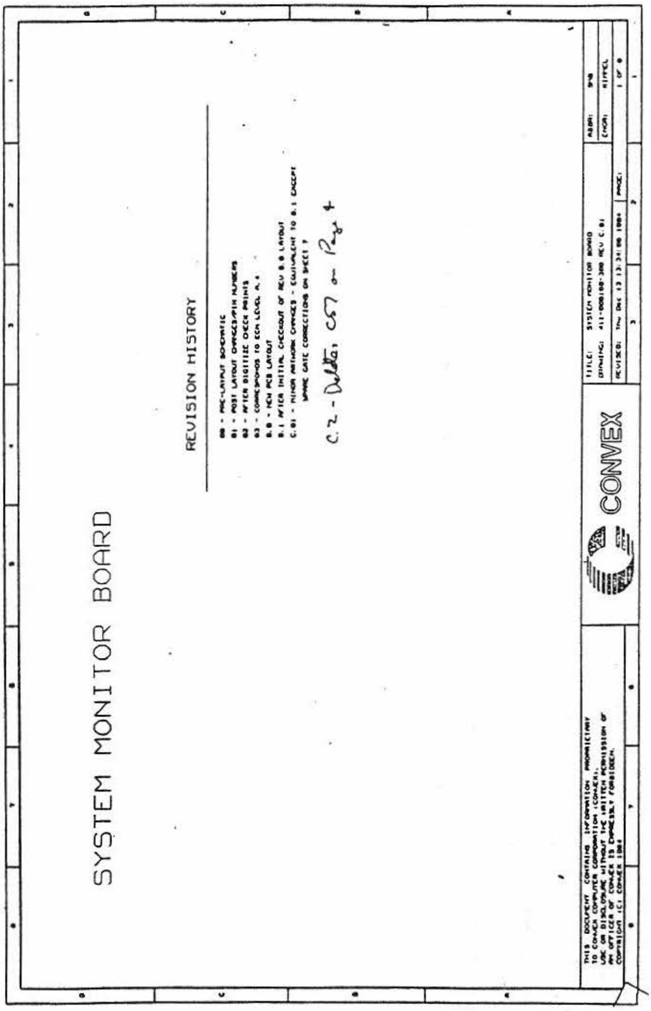
SYSTEM TYPE	SERIAL NUMBER RANGE
Standard C-1	00000 thru 04095
Rattlesnake C-1	00000 thru 04095
Junior	04096 thru 08191
Oreo	08192 thru 16383
Not assigned	16384 thru 65535

Field Support Tech Tip

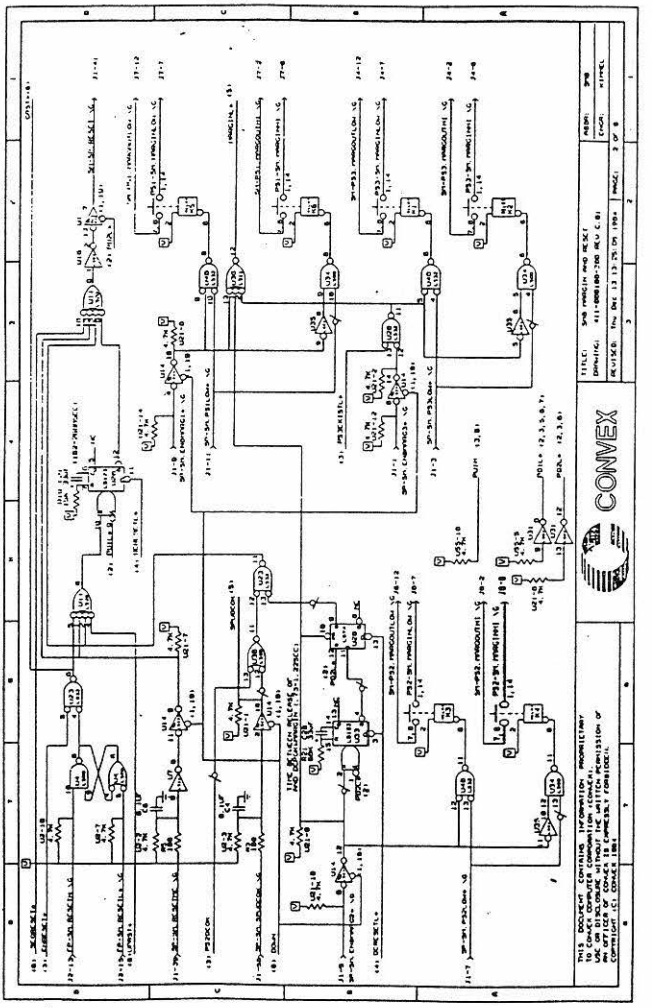
CONVEX

Product: C-1
Tech Tip Number: CPU-008
Date: March 1, 1987
Subject: System Monitor Board Prints
Submitted By: Brad Jones

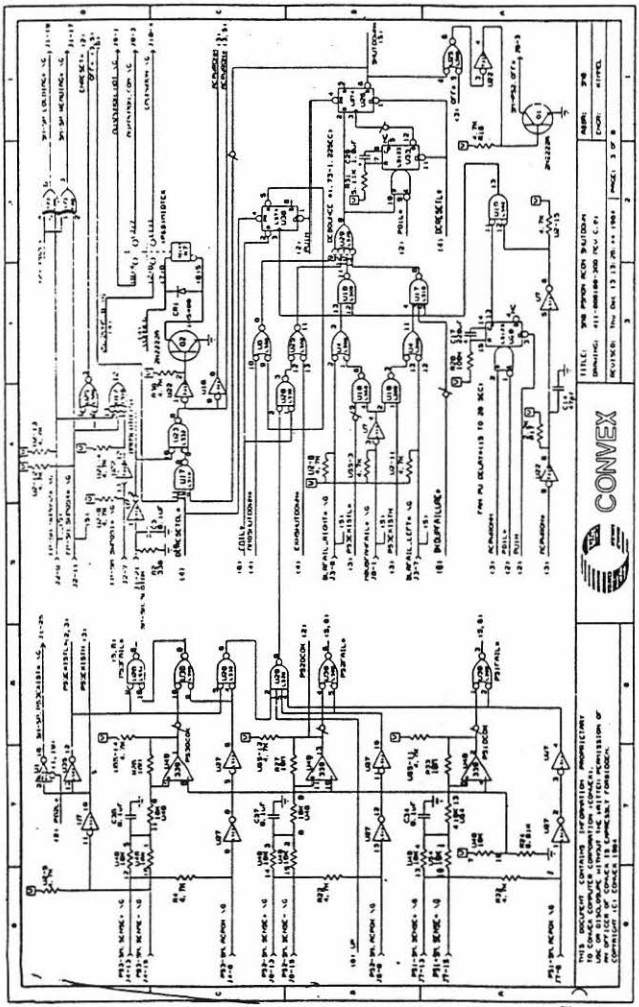
SYSTEM MONITOR BOARD P/N 411-000108-200



SYSTEM MONITOR BOARD P/N 411-000108-200 (REV. C.02)



SYSTEM MONITOR BOARD P/N 411-000108-200 (REV. C.02)

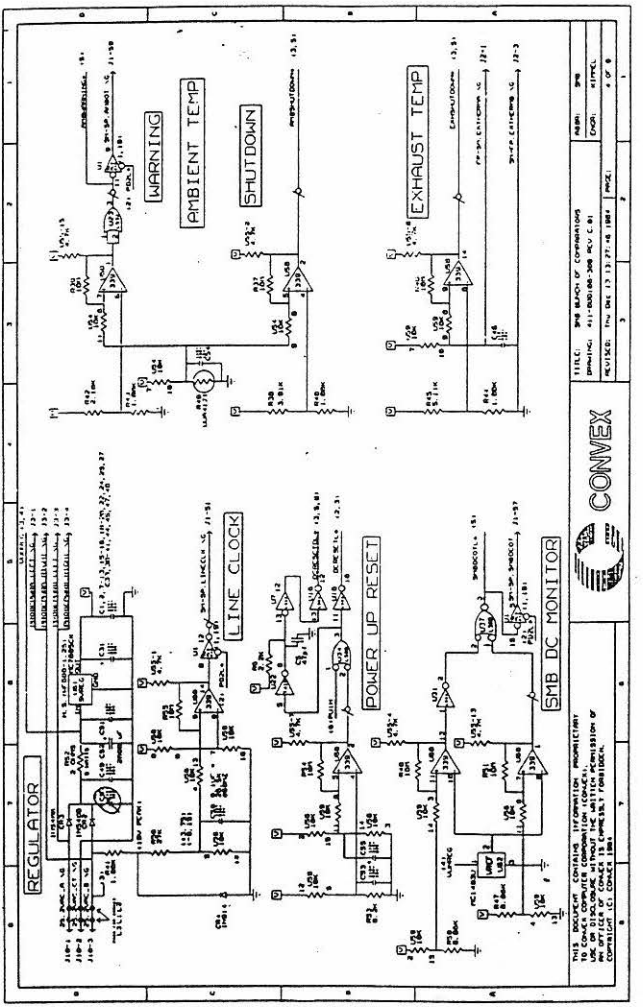


CONVEX

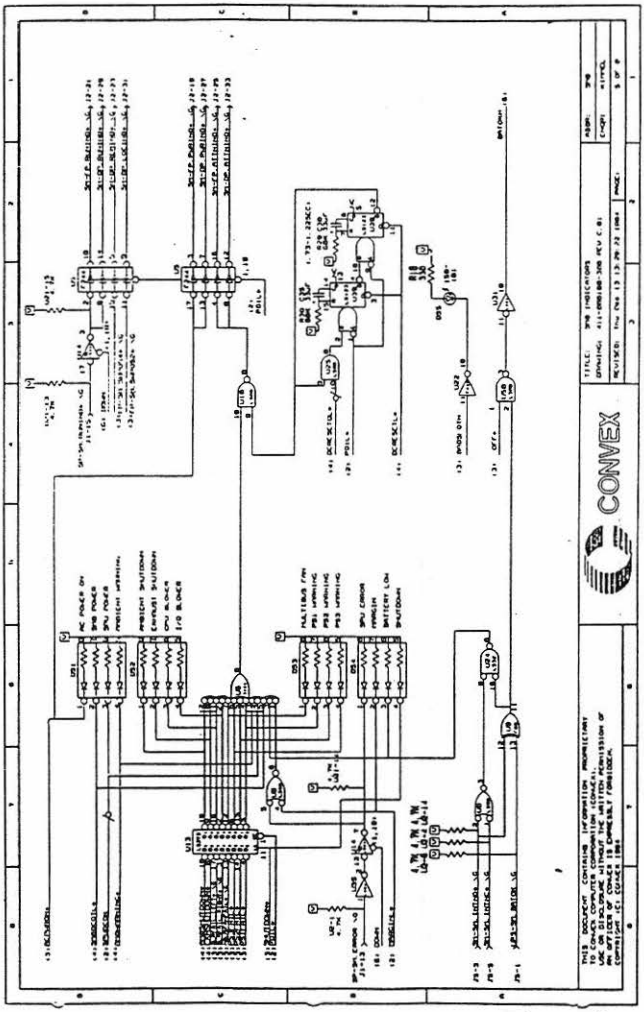
Field Support Tech Tip

Tech Tip Number: CPU-008

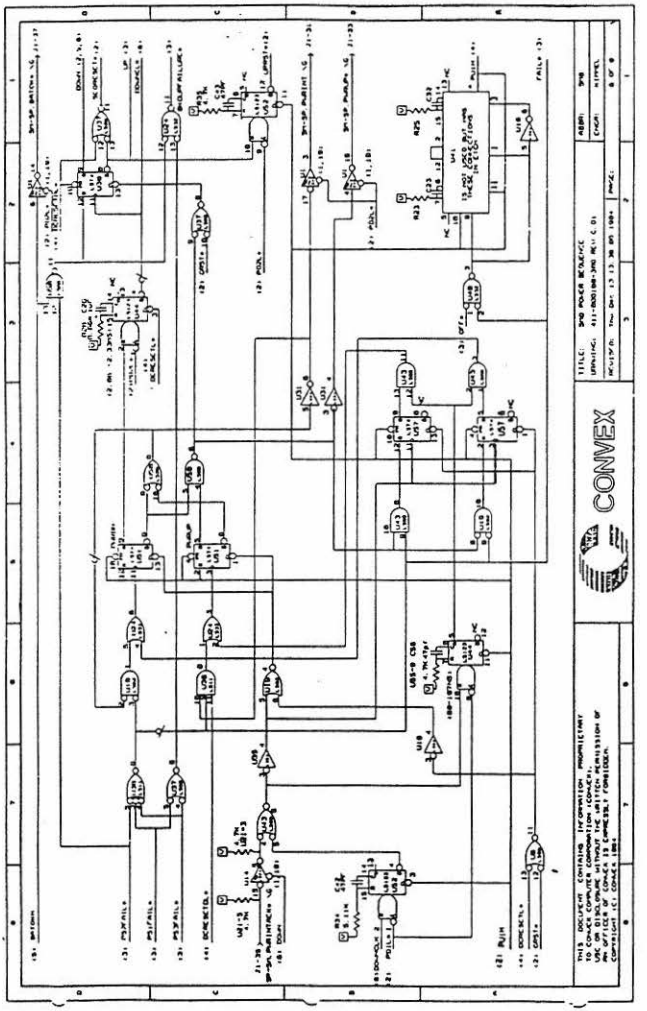
SYSTEM MONITOR BOARD P/N 411-000108-200 (REV. C.02)



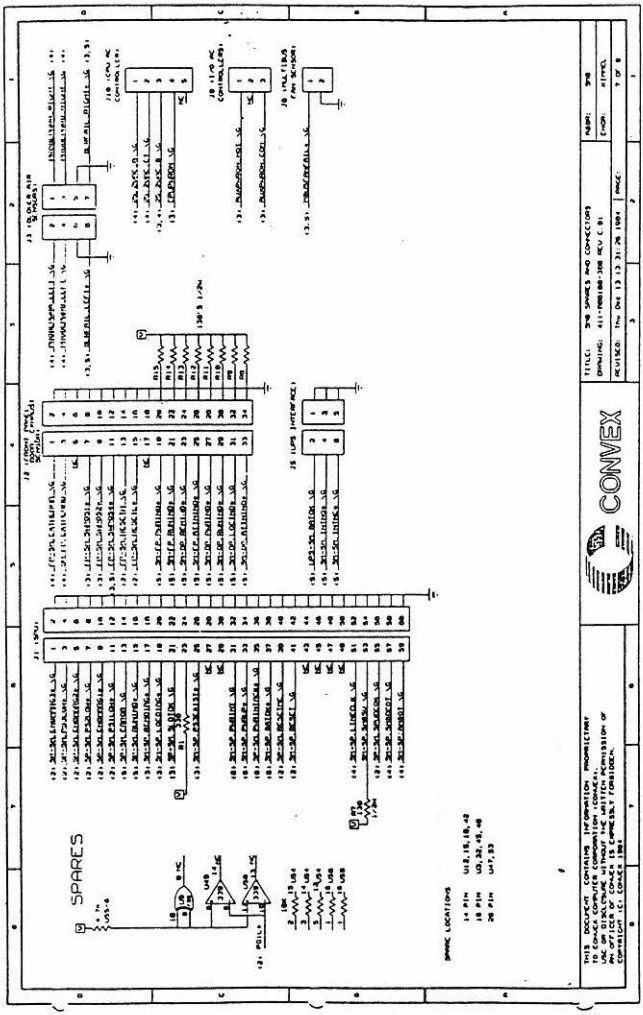
SYSTEM MONITOR BOARD P/N 411-00010B-200 (REV. C.02)



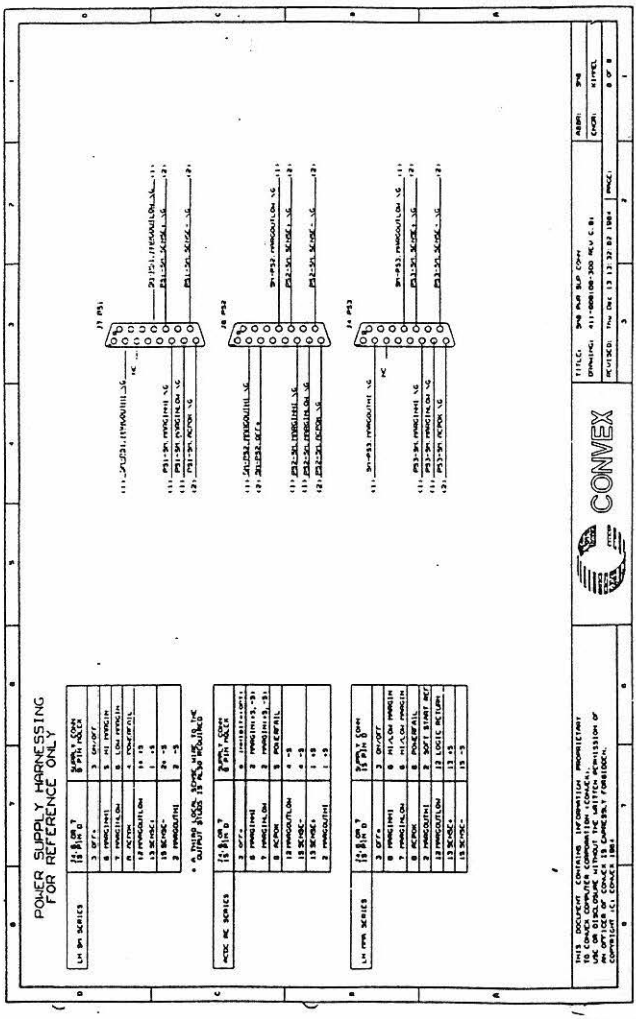
SYSTEM MONITOR BOARD P/N 411-000108-200 (REV. C.02)



SYSTEM MONITOR BOARD P/N 411-000108-200 (REV. C.02)



SYSTEM MONITOR BOARD P/N 411-000108-200 (REV. C.02)



CONVEX

Field Support Tech Tip

Product: C-1
Tech Tip Number: CPU-009
Date: February 16,1987
Subject: System Timers for C1
Submitted By: Don Davis

Overview of System Timers

General

The following is a general discussion of the timers in the C1 system with the majority of the input coming from Alan Gant and Doug Hosking. They have done a very good job at puting into perspective the interaction of the System Timers and how they are used.

SPU

(Powered Down Condition)
The SPU contains a clock timer device which is mounted on the PCB and performs the time keeping function (Refer to page 2-16 of the Convex C1 Supercomputer System Overview). When the System is powered down the SPU clock runs from a battery and uses the crystal internal to the clock device.

(Powered Up Condition)
When the SPU is powered up the clock gets its time base source from the line frequency.

NOTE: Line frequency was chosen because the frequency tolerance maintained by the power companies is 1% or less and has an averaging effect which is not a property of crystals.

(Synchronization)
The SPU code updates its idea of the time/date from a line frequency clock. Special code was required for 50 hz systems. The SPU code syncronizes the SPU time and the battery time at midnight each day.

(At Boot Time)
At boot time the SPU date/time is passed to the JP through a location in main memory page 0.

JOB PROCESSOR

There is a 2 Mhz signal which the ASU uses to drive the interval timer. The JP is interrupted every 10 ms. by the interval timer. The interrupt handler code increments the internal time by 10 ms. each time.

CONCLUSION

By understanding the methodology used in keeping time in the C1 System it will be easier to analyze timing problems and diagnose properly the symptoms of a malfunctioning system. Thanks again to Alan Gant and Doug Hosking for the information.

CONVEX

Field Support Tech Tip

Product: C-1
Tech Tip Number: CPU-010
Date: March 30, 1987
Subject: Diagnostic 'cpu4040'
Submitted By: Brad Jones

Running Diagnostic 'cpu4040' (Vector Concurrency Test) with the *default* options can take many hours. In addition, if the problem is vague, intermittent, etc., there is no guarantee that it will be worthwhile to run 'cpu4040' at all; much less for several hours.

The following sequence of inputs to 'cpu4040' will provide the parameters necessary to exercise most of the VCU/VPU registers, paths, etc. in a total time frame of less than 25 minutes (standard C-1) or less than 20 minutes (rattlesnake).

: **test cpu4040 -s 20(cr)**

```
 1.  Run default switches? [y,n]                          (y)  ->  n(cr)
 2.  SW test mode? [y,n]                                  (n)  ->  (cr)
 3.  Debugger on? [y,n]                                   (y)  ->  (cr)
 4.  Forced fail enable? [y,n]                            (n)  ->  (cr)
 5.  Main memory load verification? [y,n]                 (n)  ->  (cr)
 6.  Force display of all regs on error? [y,n]            (n)  ->  (cr)
 7.  Display update mode [f,n]                            (f)  ->  (cr)
 8.  Test display mode? [s,l]                             (s)  ->  (cr)
 9.  Lcache enabled? [y,n]                                (y)  ->  (cr)
10.  Icache enabled? [y,n]                                (y)  ->  (cr)
11.  Pcache enabled? [y,n]                                (y)  ->  (cr)
12.  Virtual memory enabled? [y,n]                        (y)  ->  (cr)
13.  Continuous faulting enabled? [y,n]                   (n)  ->  (cr)
Current group indexes:
                Group:0[0-35]          (0)>  (cr)
                Group:1[0-38]          (0)>  (cr)
                Group:2[0-40]          (0)>  (cr)
15.  Continuous loop enabled? [y,n]                       (n)  ->  (cr)
16.  Enter number of vl values to check [0-30]            (3)  ->  1(cr)
Current set of vl values:
                Vl:0 [0-128]      (32)>  128(cr)
18.  Enter number of vs values to check [0-4]             (2)  ->  1(cr)
Current set of vs for words and singles:
                vs:0 [0-33]            (4)>  33(cr)
Current set of vs for longs and doubles:
                vs:0 [0-33]            (8)>  33(cr)
21.  Input OK, or to question :nn ? [OK]                  (OK) ->  (cr)
```

- Subtest 20 will execute at this time. -

CONVEX

Field Support Tech Tip

Product: C-1
Tech Tip Number: CPU-011
Date: July 15, 1987
Subject: ASU, FASU, & DDB
Submitted By: Brad Jones

In September 1986 Diagnostic Database (DDB) Version 2.1 was released. Version 2.1 was required to support the FASU (P/N 410-001134-200) and FIPU (P/N 410-001135-200) boards; more commonly known as *Rattlesnake* (Fast Scalar). Prior to release of DDB Version 2.1, the latest usable DDB was Version 1.12 which supported the ASU (P/N 410-001129-200) and IPU (P/N 410-001126-200); commonly known as the *Standard C-1* (4 MIPS). The decision was also made that all machines shipped after September 1986, w hether *Standard* or *Rattlesnake*, would have DDB Version 2.1 or later installed. That left the existing installed customer base, each of which had either DDB Version 1.7, 1.9, 1.10, 1.11, or 1.12 in use (1.13 is also available as of this writing).

Pre-requisites and co-requisites aside, the decision whether to use DDB Version 1.13 or earlier or 2.1 or later must be based upon *system performance* considerations. Naturally, a system with the Rattlesnake boards and DDB Version 2.1 or later offers greater throughput than a system with the standard ASU and DDB Version 1.13 or earlier. Also, a system with the Rattlesnake boards must utilize DDB Version 2.1 or later if it is to work at all. However, the connection between the DDB version and the standard ASU board is not as rigid, because both DDB Version 1.13 or earlier and 2.1 or later will work with the standard ASU board.

Major DDB differences are as follows:

- A system which has the standard ASU and DDB Version 2.1 or later installed is, depending on application, at risk of running slower than it would if DDB Version 1.13 or earlier was installed. This is due to the methods used by each to perform *convert* instructions.
- DDB Version 1.13 or earlier *truncates* a floating point result and DDB Version 2.1 or later uses a *rounding* algorithm that is more accurate. This means that two different machines can come up with a different answer to an identical problem if one uses DDB Version 1.13 or earlier and the other uses DDB Version 2.1 or later.

Therefore, if DDB Version 2.1 or later is installed on a Standard C-1, it must be realized that more correct answers will be obtained, but system throughput may suffer.

The system throughput issue is the reason that DDB Version 1.13 and earlier is still available. If DDB Version 2.1 or later is installed on a Standard C-1 and system throughput suffers, a (free?) Rattlesnake upgrade would be required to correct the problem.

CONVEX

Field Support Tech Tip

Product: C-1
Tech Tip Number: CPU-012
Date: October 2,1987
Subject: Pin-out for XL/XE
Submitted By: Don Davis

Pin-out for Remote Connector on XL/XE

General

Remote Control Pinout for XE & XL C1 Configurations

A 15 pin male "D-shell" connector labeled "Control" is provided on the rear bulkhead of the XE/XL chassis configuration. This connector allows, via an external cable, access to the following CPU control functions:

1. Power On/Off
2. Local Maintenance Enable
3. Remote Maintenance Enable
4. System Reset
5. Attention Status

Pinout of the Remote connector follows:

	o-1 GND	
9-o	SWPOS2*	(LOCAL MAINTENANCE)
	o-2 GND	
10-o	SWPOS1*	(OFF)
	o-3 GND	
11-o	SWPOS4*	(REMOTE MAINTENANCE)
	o-4 GND	
12-o	ATTNIND*	
	o-5 GND	
13-o	RESETH	
	o-6 N/C	
14-o	RESETL*	
	o-7 N/C	
15-o	N/C	
	o-8 N/C	

Notes:

1. All inputs must be driven by a device with a minimum 3mA sinking capacity.

2. Attention indicator output will sink a maximum of 16mA at a low level output voltage of 0.4 volts.

CONVEX

Field Support Tech Tip

Product: C-1
Tech Tip Number: CPU-012a
Date: October 2,1987
Subject: Pin-out for XL/XE
Submitted By: Don Davis

OPERATION DETAILS -

For remote operation the keylock on the front panel of the XE/XL chassis must be left in the "Secure Operation" position and the front panel reset switch must be disconnected from the front panel board. (Note: Consult Convex service representive for details)
Connection to the Control connector should be made using a full 360 degree shielded cable to prevent radiated emissions.
(Amp mating connector P/N 205205-2 or equivalent)
The following is a description of the implementation of the above functions respectively:

1. An open or TTL compatible voltage above 2.0 volts on pin 10 will turn the machine on. A ground or TTL voltage below 0.4 volts on pin 10 will turn the machine off.

2. Once the machine is turned on, a ground or TTL voltage below 0.4 volts on pin 9 will enable the Local Maintenance mode. An open or TTL compatible voltage above 2.0 volts on pin 9 will disable Local Maintenance. (Note: Local and Remote Maintenance modes are mutually exclusive and should not be enabled simultaneously)

3. Once the machine is turned on, a ground or TTL voltage below 0.4 volts on pin 11 will enable the Remote Maintenance mode. An open or TTL compatible voltage above 2.0 volts on pin 11 will disable Remote Maintenance. (Note: Local and Remote Maintenace modes are mutually exclusive and should not be enabled simultaneously)

4. A momentary single pole double throw switch - Normally Open connected to RESETL*(pin 14), Normally Closed connected to RESETH (pin 13), and Pole connected to GND(pin 1-5) - will issue a RESET to the system when depressed.

5. When a condition exists that requires operator attention, Pin 12 will pulse at TTL levels at approximately 1Hz. frequency.

Descriptions of the above controls and a summary of the "Attention" conditions can be referenced in the system managers guide Convex P/N 710-000030-000.

CONVEX

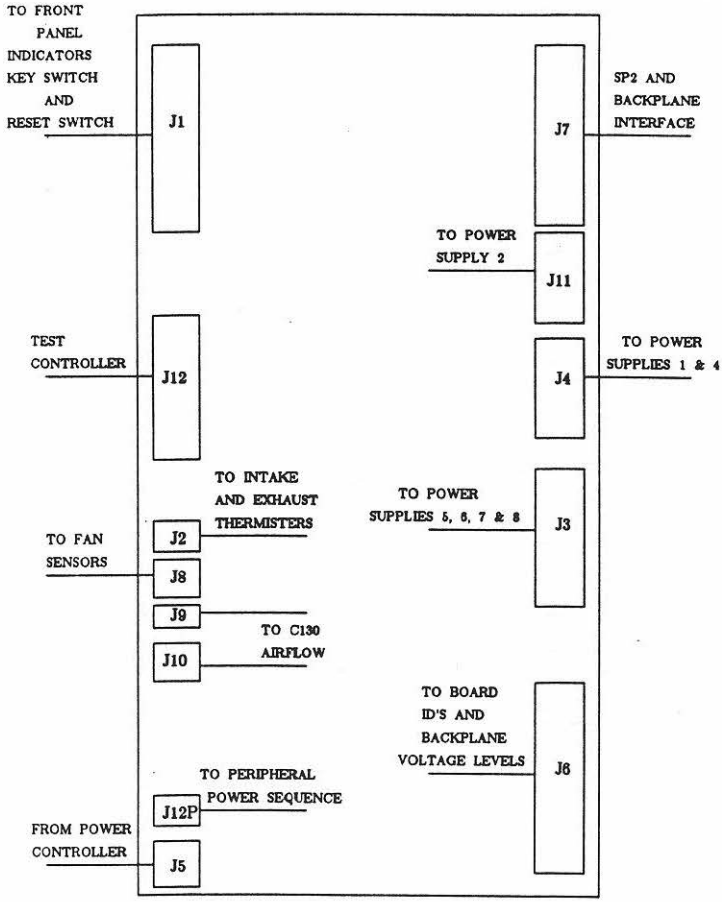
Field Support Tech Tip

Product: C210/220
Tech Tip Number: cpu-013
Date: December 8,1988 Rev 12/31/89
Subject: C210/220 SCM CONNECTORS
Submitted By: A.Clark/Ray

SCM CONNECTOR DEFINITION

SCM Board Connectors	Cable Destination	Cable Part Number
J1	Front Panel J1	601-600002-202
J2	Thermisters	603-100001-200
J3	PS 5, 6, 7, 8	603-320001-200
J4	PS 1, 4	603-320002-200
J5	AC power from PCU	603-640014-200
J6	Backplane J15	601-600016-200
J7	Backplane J14	601-640001-200
J8	Fan sensors	603-100001-200
J9	ID connector	
J10	Not used	
J11	PS 3	603-320002-200
J12	Test controller	
J12P	I/O power sequencer	

SCM BOARD CONNECTORS



SCM CONNECTOR - J1

PIN	FROM	TO	SIGNAL
1			VCC_EXT
2			GROUND
3	SCM	FP	PS20K
4			GROUND
5	SCM	FP	PS30K
6			GROUND
7	SCM	FP	PS40K
8			GROUND
9	SCM	FP	PS50K
10			GROUND
11	SCM	FP	PS60K
12			GROUND
13	SCM	FP	PS70K
14			GROUND
15	SCM	FP	PS80K
16			GROUND
17	SCM	FP	ATTNIND
18			GROUND
19	SCM	FP	PWRIND
20			GROUND
21	SCM	FP	RUN
22			GROUND
23	SCM	FP	CPU1IDLE
24			GROUND
25	SCM	FP	CPU2IDLE
26			GROUND
27	FP	SCM	PWROFF
28			GROUND
29	FP	SCM	LOCDIAG
30			GROUND
31	FP	SCM	REMDIAG
32			GROUND
33	FP	SCM	RESET
34			GROUND
35	FP	SCM	REMIND
36			GROUND
37	FP	SCM	PWRIND
38			GROUND
39	FP	SCM	RUNIND
40			GROUND
41	FP	SCM	LOCIND
42			GROUND
43	FP	SCM	ATTNIND
44			GROUND
45	SCM	FP	HEXDISP 0
46			GROUND
47	SCM	FP	HEXDISP 1
48			GROUND
49	SCM	FP	HEXDISP 2
50			GROUND
51	SCM	FP	HEXDISP 3
52			GROUND
53	SCM	FP	HEXDISP 4
54			GROUND
55	SCM	FP	HEXDISP 5
56			GROUND
57	SCM	FP	HEXDISP 6
58			GROUND
59	SCM	FP	HEXDISP 7
60			VCC_EXT

SCM CONNECTOR - J2

PIN	FROM	TO	SIGNAL
1	TS1	SCM	THERMIN
2	TS1	SCM	THERMGND
3	TS2	SCM	THERMIN
4	TS2	SCM	THERMGND

SCM CONNECTOR - J3

PIN	FROM	TO	SIGNAL
1	PS5	SCM	ISHAR
2			GROUND
3	PS5	SCM	MARGIN +
4	PS5	SCM	MARGOUT +
5	PS5	SCM	MARGIN -
6	PS5	SCM	MARGOUT -
7	SCM	PS5	ON_CMDMB
8	SCM	PS5	ON_BIAS
9	PS5	SCM	ACPOK
10			GROUND
11	PS5	SCM	XIST
12			GROUND
13	PS6	SCM	ISHAR
14			GROUND
15	PS6	SCM	MARGIN +
16	PS6	SCM	MARGOUT +
17	PS6	SCM	MARGIN -
18	PS6	SCM	MARGOUT -
19	SCM	PS6	ON_CMD
20	SCM	PS6	ON_BIAS
21	PS6	SCM	ACPOK
22			GROUND
23	PS6	SCM	XIST
24			GROUND
25	PS7	SCM	ISHAR
26			GROUND
27	PS7	SCM	MARGIN +
28	PS7	SCM	MARGOUT +
29	PS7	SCM	MARGIN -
30	PS7	SCM	MARGOUT -
31	SCM	PS7	ON_CMD
32	SCM	PS7	ON_BIAS
33	PS7	SCM	ACPOK
34			GROUND
35	PS7	SCM	XIST
36			GROUND
37	PS8	SCM	ISHAR
38			GROUND
39	PS8	SCM	MARGIN +
40	PS8	SCM	MARGOUT +
41	PS8	SCM	MARGIN -
42	PS8	SCM	MARGOUT -
43	SCM	PS8	ON_CMD
44	SCM	PS8	ON_BIAS
45	PS8	SCM	ACPOK
46			GROUND
47	PS8	SCM	XIST
48			GROUND
49	NOT USED		
50	NOT USED		

SCM CONNECTOR - J5

PIN	FROM	TO	SIGNAL
1	24VAC_A		
2	24VAC_CT		
3	24VAC_B		
4	CPUPWRON		

SCM CONNECTOR - J8

PIN	FROM	TO	SIGNAL
1			VCC_EXT
2			VCC_EXT
3			GROUND
4			GROUND
5			FN0-SCM
6			FN3-SCM
7			FN1-SCM
8			FN4-SCM
9			FN2-SCM
10			FN5-SCM

SCM CONNECTOR - J4

PIN	FROM	TO	SIGNAL
1	PS1	SCM	ISHAR
2			GROUND
3	PS1	SCM	MARGIN +
4	PS1	SCM	MARGOUT +
5	PS1	SCM	MARGIN -
6	PS1	SCM	MARGOUT -
7	SCM	PS1	ON_CMD
8	SCM	PS1	ON_BIAS
9	PS1	SCM	ACPOK
10			GROUND
11	PS1	SCM	XIST
12			GROUND
13	PS4	SCM	ISHAR
14			GROUND
15	PS4	SCM	MARGIN +
16	PS4	SCM	MARGOUT +
17	PS4	SCM	MARGIN -
18	PS4	SCM	MARGOUT -
19	SCM	PS4	ON_CMD
20	SCM	PS4	ON_BIAS
21	PS4	SCM	ACPOK
22			GROUND
23	PS4	SCM	XIST
24			GROUND
25	NOT USED		
26	NOT USED		
27	NOT USED		
28	NOT USED		
29	NOT USED		
30	NOT USED		
31	NOT USED		
32	NOT USED		
33	NOT USED		
34	NOT USED		

SCM CONNECTOR - J6

PIN	FROM	TO	SIGNAL
2			VCC (+5V DC)
4			VCC (+5V DC)
6			VEE (-4.5V DC)
8			VTT (-2V DC)
10	PIA	SCM	
12	ME0	SCM	
14	ME1	SCM	
16	ME2	SCM	
18	ME3	SCM	
20	MO0	SCM	
22	MO1	SCM	
24	MO2	SCM	
26	MO3	SCM	
28	CFX	SCM	
30	SP2	SCM	
32	ASPA	SCM	
34	IPPA	SCM	
36	SFUA	SCM	
38	DCUA	SCM	
40	VPCA	SCM	
42	VPDA	SCM	
44	ASPB	SCM	
46	IPPB	SCM	
48	SFUB	SCM	
50	DCUB	SCM	
52	VPCB	SCM	
54	VPDB	SCM	
56			+12V DC
58			-5V DC
60			-12V DC

All odd pins are grounds
Pins 61 through 64 are not used

SCM CONNECTOR - J7

PIN	FROM	TO	SIGNAL
2	SP2	SCM	data bit 0
4	SP2	SCM	data bit 1
6	SP2	SCM	data bit 2
8	SP2	SCM	data bit 3
10	SP2	SCM	data bit 4
12	SP2	SCM	data bit 5
14	SP2	SCM	data bit 6
16	SP2	SCM	data bit 7
18	SP2	SCM	DATA AVIL
20	SP2	SCM	COMM AVIL
22	SCM	SP2	SCM ACK
24	SCM	SP2	SCM DCOK
26	SP2	SCM	ERROR
28	SP2	SCM	RUNIND
30	SCM	SP2	REMDIAG
32	SCM	SP2	LOCDIAG
34	SCM	SP2	PWRINT
36	SCM	SP2	PWRUP
38	SP2	SCM	PWRINTAK
40	NOT USED		
42	SCM	SP2	PWRUP RESET
44	SCM	SP2	RESET
46	DCU	SCM	AIRFLOW
48	PIS	SCM	AIRFLOW
50	ASPA	SCM	RUNNING
52	ASPB	SCM	RUNNING
54	SCM	SP2	LINECLK
56	SP2	SCM	SFUDCOK
58	NOT USED		
60	SCM	SP2	AMBOT

Pins 61 through 64 are not used
All odd pins are ground

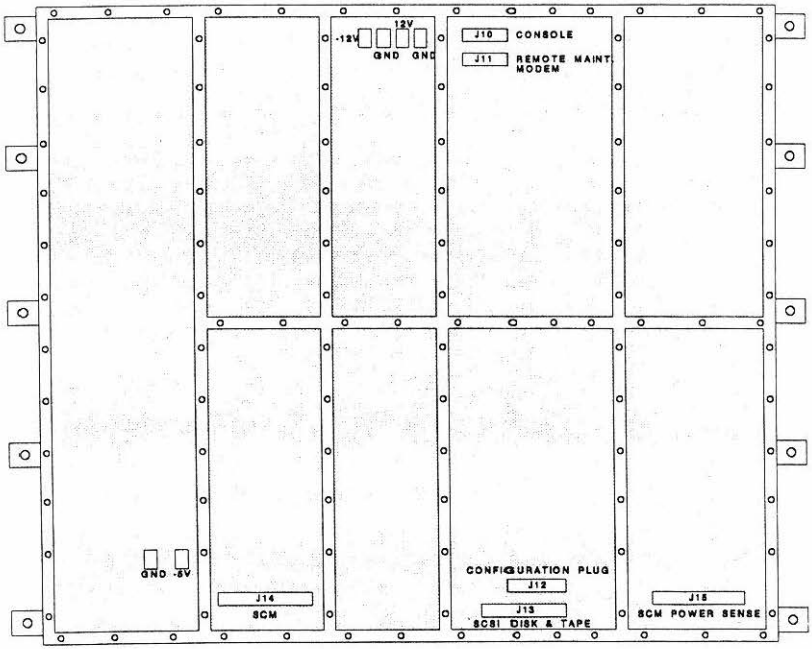
SCM CONNECTOR - J11

PIN	FROM	TO	SIGNAL
1	NOT USED		
2			GROUND
3	PS2	SCM	MARGIN +
4	PS2	SCM	MARGOUT +
5	PS2	SCM	MARGIN -
6	PS2	SCM	MARGOUT -
7	SCM	PS2	ON_CMD
8	SCM	PS2	ON_BIAS
9	PS2	SCM	APCOK
10			GROUND
11	PS2	SCM	XIST
12			GROUND
13	NOT USED		
14			GROUND
15	NOT USED		
16	NOT USED		
17	NOT USED		
18	NOT USED		
19	NOT USED		
20	NOT USED		
21	NOT USED		
22	NOT USED		
23	NOT USED		
24	NOT USED		
25	NOT USED		
26	NOT USED		

SCM CONNECTOR - J12P

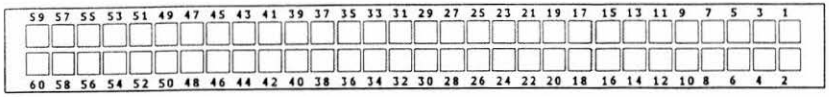
PIN	FROM	TO	SIGNAL
1	SCM	PC	PWRON
2	NOT USED		
3	SCM	PC	PWRONRET

BACKPLANE



Pin one on the backplane connectors is the top right pin from the rear of the backplane. See drawing on next page.

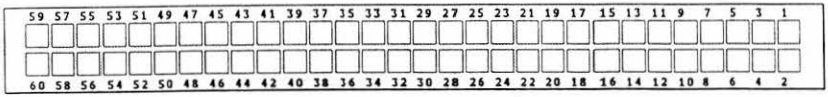
C210/220 BACKPLANE CONNECTOR J14



All odd pins are ground

2	SP2 to SCM data bit 0	22	SCM to SP2 SCM ACK	42	SCM to PIA PWRUP RESET
4	SP2 to SCM data bit 1	24	SCM to SP2 SCM DCOK	44	SCM to SP2 RESET
6	SP2 to SCM data bit 2	26	SP2 to SCM ERROR	46	DCU to SCM AIRFLOW
8	SP2 to SCM data bit 3	28	SP2 to SCM RUNIND	48	PIS to SCM AIRFLOW
10	SP2 to SCM data bit 4	30	SCM to SP2 REMDIAG	50	ASPA to SCM RUNNING
12	SP2 to SCM data bit 5	32	SCM to SP2 LOCDIAG	52	ASPB to SCM RUNNING
14	SP2 to SCM data bit 6	34	SCM to SP2 PWRINT	54	SCM to SP2 LINECLK
16	SP2 to SCM data bit 7	36	SCM to SP2 PWRUP	56	SP2 to SCM SPUDCOK
18	SP2 to SCM DATA AVAIL	38	SP2 to SCM PWRINTAK	58	NOT USED
20	SP2 to SCM COMM AVAIL	40	NOT USED	60	SCM to SP2 AMBOT

C210/220 BACKPLANE CONNECTOR J15



All odd pins are ground

2	VCC (+5V DC)	22	MO1 to SCM	42	VPDA to SCM
4	VCC (+5V DC)	24	MO2 to SCM	44	ASPB to SCM
6	VEE (-4.5V DC)	26	MO3 to SCM	46	IPPB to SCM
8	VTT (-2V DC)	28	CPX to SCM	48	SFUB to SCM
10	PIA to SCM	30	SP2 to SCM	50	DCUB to SCM
12	ME0 to SCM	32	ASPA to SCM	52	VPCB to SCM
14	ME1 to SCM	34	IPPA to SCM	54	VPDB to SCM
16	ME2 to SCM	36	SFUA to SCM	56	+12V DC
18	ME3 to SCM	38	DCUA to SCM	58	-5V DC
20	MO0 to SCM	40	VPCA to SCM	60	-12V DC

The above is from the rear of the backplane.

C210/220 BACKPLANE CONNECTOR J15

All odd pins are ground

2	VCC (+5V DC)	22	MO1 to SCM	42	VPDA to SCM
4	VCC (+5V DC)	24	MO2 to SCM	44	ASPB to SCM
6	VEE (-4.5V DC)	26	MO3 to SCM	46	IPPB to SCM
8	VTT (-2V DC)	28	CPX to SCM	48	SFUB to SCM
10	PIA to SCM	30	SP2 to SCM	50	DCUB to SCM
12	ME0 to SCM	32	ASPA to SCM	52	VPCB to SCM
14	ME1 to SCM	34	IPPA to SCM	54	VPDB to SCM
16	ME2 to SCM	36	SFUA to SCM	56	+12V DC
18	ME3 to SCM	38	DCUA to SCM	58	-5V DC
20	MO0 to SCM	40	VPCA to SCM	60	-12V DC

The above is from the rear of the backplane.

CONVEX

Field Support Tech Tip

Product: C2XX
Tech Tip Number: CPU-014
Date: August 18,1989/Rev 02/10/90
Subject: C2 VEE,VTT & VCC CNTL
Submitted By: TAC - HW

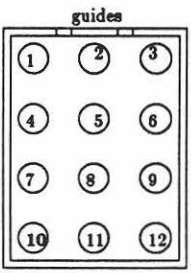
VEE & VTT CONNECTORS on the POWER SUPPLIES

The following drawing and chart will illustrate the pin numbers and signals in the VEE and VTT (white) connectors on all the power supplies.

Special care must be taken on how the connectors are plugged in the power supplies. The connector's orientation can be determined by the placement of the two(2) connector guides.

PIN	PS-1 COLOR	PS-4 COLOR	PS-5 COLOR	PS-6 COLOR	PS-7 COLOR	PS-8 COLOR	SIGNAL
1	RED	ORANGE	RED	ORANGE	YELLOW	GREEN	GND-REF
2	ORANGE	YELLOW	ORANGE	YELLOW	GREEN	BLUE	MARGIN+
3	YELLOW	GREEN	YELLOW	GREEN	BLUE	VIOLET	MARGOUT+
4	GREEN	BLUE	GREEN	BLUE	VIOLET	GREY	MARGIN-
5	WHITE	BLACK	WHITE	BLACK	BROWN	RED	ACPOK
6	GRAY	WHITE	GRAY	WHITE	BLACK	BROWN	ON_BIAS
7	VIOLET	GRAY	VIOLET	GRAY	WHITE	BLACK	ON_CMD
8	BLUE	VIOLET	BLUE	VIOLET	GRAY	WHITE	MARGOUT-
9							
10	BROWN	RED	BROWN	RED	ORANGE	YELLOW	IMON
11	BLACK	BROWN	BLACK	BROWN	RED	ORANGE	GND_BIAS
12	BROWN	RED	BROWN	RED	ORANGE	YELLOW	XIST*

TOP VIEW - WIRE SIDE

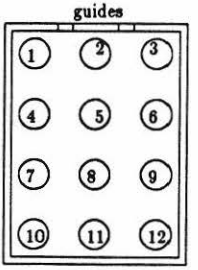


Pin 10 on this connector is useful when determining whether a power supply is not carrying its portion of the current share. Meter **Red** lead on VEE or VTT at the backplane and **Black** lead to pin 10. Normally all slave supplies will indicate within 0.1 vdc of each other and the master indicating somewhat higher. If one slave is much lower and the master is much higher, this indicates that the slave exceeded tolerance and the master responded to make up the lost load. If all slaves appear to be in tolerance with each other, the master is probably at fault.

VCC CONNECTOR on the POWER SUPPLY

PIN	PS-1 COLOR	SIGNAL
1	RED	GND
2	ORANGE	MARGIN_IN+
3	YELLOW	MARGIN_OUT+
4	GREEN	MARGIN_IN-
5	BLUE	ACPOK
6	VIOLET	ON_BIAS
7	GRAY	ON_CMD
8	WHITE	MARGIN_OUT-
9		
10		
11	BLACK	PF-
12	BROWN	XIST*

TOP VIEW - WIRE SIDE



CONVEX

Field Support Tech Tip

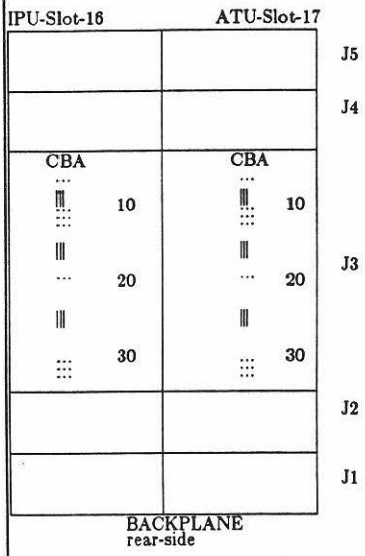
Product: C-1
Tech Tip Number: CPU-015
Date: July 31, 1989
Subject: Restoral of backplane
Submitted By: Gerry Palmer

There may be cases where there is not a current rev ATU and FIPU available and it is necessary to use a lower rev ATU or IPU to get the customer up temporarily while waiting for the proper revision boards.

In order to install the rev C FIPU, rev U IPU and rev S ATU it was necessary to upgrade the backplane on a C1 to rev E. To do this FMI 0049 was released, which required a wire be added between ATU J3 B12 and IPU J3 B17.

To return backplane to a condition suitable for installing these lower rev boards is a fairly simple operation and detailed below:

To use an OLD ATU (below Rev S) then add B/P wire from ATU J3 A32 to ATU J3 B12. To use an OLD IPU (below Rev U) then add B/P wire from IPU J3 A32 to IPU J3 B17.



CONVEX

Field Support Tech Tip

Product: C-1
Tech Tip Number: CPU-016
Date: November 2, 1989
Subject: Memory Interleave
Submitted By: Harold Lewis

C-1 MEMORY INTERLEAVE ABOVE 4

If the memory in a C1 is being increased to achieve an interleave of more than 4, ensure that the MCU and PCU are taken in to consideration.

****** NOTE ******
The MCU **MUST** be a 410-001136-200
The PCU **MUST** be a 410-001137-200.

If these two boards are not installed in the system, an interleave of 4 is all that will be allowed. This is controlled by SPU UNIX.

C1 MEMORY INTERLEAVE

C1 memory interleave above 4 requires both MCU 410-1136-200 and PCU 410-1137-200 to be present in the system. The resultant interleave is a function of two things:

1) All MAUs must be the same size (all 16 MB, all 32 MB, or all 128 MB) to achieve greater than 4-way interleave

2) If all MAUs are the same size, then the interleave obtained is a function of the number of MAUs:

# of MAUs	Interleave
1	4
2	8
3	4
4	16
5	4
6	4
7	4
8	32

Four way interleave is achieved by switching between the four memory banks present on each MAU. Interleaves greater than 4 are achieved by switching between MAUs. In order for this scheme to work, the number of MAUs present must be a power of two. Otherwise, only 4-way interleave is obtainable.

CONVEX

Field Support Tech Tip

Product: MCM2
Tech Tip Number: CPU-017
Date: 1/10/90
Subject: MIM Location Decoding
Submitted By: Dave Muir

MCM2 Information and MIM Decoding

The MCM2 is configured with 128 MB of storage on a single memory board. This allows Convex to offer up to 1GB of real memory in the C2 systems.

A few early MCM2's were shipped with the MIM (the small pcb containing the memory chips) soldered to the main board. As a result the MIM's on these boards cannot be changed in the field.

The newer boards will have the ground clip soldered to the MIM at one end. This will make sure there is a solid ground contact from the MIM and the MCM2 mother board. When a defective MIM is removed and a new MIM installed, be sure to solder the ground clip to the board.

The MCM2 must be handled with more care than other memory boards in order to prevent damage to the MIM's or the connectors. These connectors are susceptible to breakage or damage if mis-handled during installation, removal or packing the module for shipment.

The profile of the MCM2 is higher than the earlier memories. This means that any system using MCM2's must be used in the C240 wide body cabinet. Keep this in mind when doing pre-site audits for new systems.

MCM2 part numbers:

550-000199-200	MCM2 128mb
410-001226-200	MCM2 without MIM 's
411-000186-200	MCM2 MIM

Using the data in the sample errlog and MIM selection matrix, a defective MIM can be located. Note that the information in the DEVICE column of the softlog is not applicable to the MCM2, and the MIM selection matrix must be used.

The chart on the next page can be used to decode failing addresses using information from any failure log or diagnostic error output, however, the failing bit must be known to decode down to the MIM.

Sample failure log.

```
M              MCM       B S
C              SERIAL    I T
M    DEVICE    NUMBER    T K     FIRST FAIL              LAST FAIL               ADDR    #FAILS
--  --------- --------  -- - ----------------- ----------------- -------- ------
LATEST FAILURE:
0e LR-U023H8  00530798 29    Nov 12 18:20 1989 Nov 12 18:20 1989 33512708 000001
EARLIEST FAILURE:
0e UR-Z031B0  00530798  1    Oct  1 22:16 1989 Oct  1 22:16 1989 3022ce38 000001
LOGGED FAILURES:
0e UR-Z031B0  00530798  1    Oct  1 22:16 1989 Oct  1 22:16 1989 3022ce38 000001
1e UR-U006K4  00530825 C1    Oct 15 14:01 1989 Oct 15 14:01 1989 30174be8 000001
0e LR-U023H8  00530798 29    Nov 12 18:20 1989 Nov 12 18:20 1989 33512708 000001
```

Using the data from the LATEST FAILURE the error is decoded as follows:

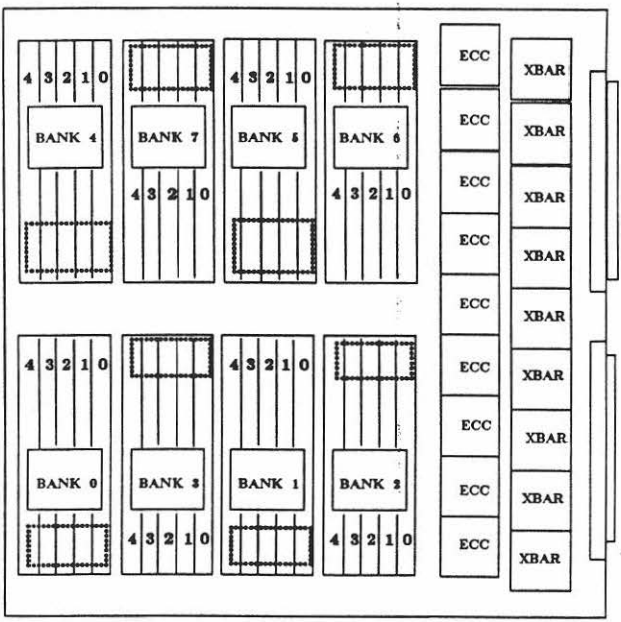
```
                          (ADDR)
   Failing address --->  33512708
                                ||  Use bit 6 only for 1 or 2 board pairs
                          ______||  Use bits 6 & 7 for 4 board pairs
                         |      |
     7    6    5    4   |  3   2    1    0      BD = Board Pair
    BD   BD   BK   BK   | BK  E/O  BT   BT      BK = Bank Number
    ------------------------------------------  E/O = Even/Odd Board
            0            |        8             BT = Byte Number
    ------------------------------------------
     0    0    0    0   |  1   0    0    0
    ------------------------------------------

This address = Board Pair -  0
               Bank Number - 1
               E/O Board   - E
```

MIM selection matrix

Data Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIM	4	4	4	4	4	4	3	3	3	3	3	3	2	2	2	2
Data Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MIM	2	2	1	1	1	1	1	1	0	0	0	0	0	0	0	0

ECC Bits	6	5	4	3	2	1	0
MIM	4	3	3	2	2	1	1

MCM2


4 3 2 1 0
BANK 4
4 3 2 1 0
BANK 7
4 3 2 1 0
BANK 5
4 3 2 1 0
BANK 6
4 3 2 1 0
BANK 0
4 3 2 1 0
BANK 3
4 3 2 1 0
BANK 1
4 3 2 1 0
BANK 2
ECC
ECC
ECC
ECC
ECC
ECC
ECC
ECC
ECC
XBAR
XBAR
XBAR
XBAR
XBAR
XBAR
XBAR
XBAR
XBAR

CONVEX

Field Support Tech Tip

Product: C-2
Tech Tip Number: CPU-018
Date: February 20, 1990
Subject: Head Disable Procedure
Submitted By: Al Haddix

We have, frequently, been asked if there is a method of disabling a head from the OS. The answer to this question is yes. It is important that you understand that what follows will only disable the head from on-line execution, but because microcode is still loaded on the head it still may participate in background activities.

While this may be of help in diagnosing application related problems, it is probably of little use in troubleshooting hard errors.

The utility to disable the head from executing any process is called "cpuconf". The primary switches are -ecpunumber and -dcpunumber. Example: "cpuconf -d1" will disable head 1.

The utility mpa can be used to restrict a single specific process from running on the given head. Example "mpa -c2" will disable this process from running on head 2. The -c option is only available with version 7.1 of the OS.

If you wish to know more about these utilities, a man page exists for both mpa and cpuconf.

Field Support Tech Tip

Product: C-2
Tech Tip Number: CPU-019
Date: February 28, 1990
Subject: C210/220 SCM Status
Submitted By: Al Haddix

SCM Error and Message Codes
firmware revision 1.18

Code	Error/ Message
00	Deadman timer indicates scm internal problem
02	SP-SM.PWRINTAK* failure
04	SP-SM.smbdata<7..0>* failure
07	SP-SM.SPUDCOK failure
0B	SP2/SP4 invalid command code
10	ME0 installed incorrectly
11	MO0 installed incorrectly
12	ME1 installed incorrectly
13	MO1 installed incorrectly
14	ME2 installed incorrectly
15	MO2 installed incorrectly
16	ME3 installed incorrectly
17	MO3 installed incorrectly
18	CPX installed incorrectly
19	VPDA installed incorrectly
1A	VPDB installed incorrectly
1B	PIA installed incorrectly
1C	SP2 installed incorrectly
1D	SFUA installed incorrectly
1E	SFUB installed incorrectly
1F	ASPA installed incorrectly
20	ASPB installed incorrectly
21	IPPA installed incorrectly
22	IPPB installed incorrectly
23	VPCA installed incorrectly
24	VPCB installed incorrectly
25	DCUA installed incorrectly
26	DCUB installed incorrectly
81	PS1 AC power failure
82	PS2 AC power failure
83	PS3 AC power failure
84	PS4 AC power failure
85	PS5 AC power failure
86	PS6 AC power failure
87	PS7 AC power failure
88	PS8 AC power failure
89	+5V DC power supply failure
8A	+12V DC power supply failure
8B	-12V DC power supply failure

SCM Error and Message Codes (cont) firmware revision 1.18	
Code	Error/ Message
8C	-5V DC power supply failure
8D	-4.5V DC power supply failure
8E	-2V DC power supply failure
91	PS1 exceeds maximum rated current
94	PS4 exceeds maximum rated current
95	PS5 exceeds maximum rated current
96	PS6 exceeds maximum rated current
97	PS7 exceeds maximum rated current
98	PS8 exceeds maximum rated current
A9	+5V voltage not within tolerance
AA	+12V voltage not within tolerance
AB	-12V voltage not within tolerance
AC	-5V voltage not within tolerance
AD	-4.5V voltage not within tolerance
AE	-2V voltage not within tolerance
B0	Excessive intake temperature/ sensor fault
B1	Excessive exhaust temperature/ sensor fault
B4	CPX airflow failure
B5	PIA airflow failure
B6	SCM thermister fault
C0	Insufficient power supplies for board configuration
D1	PS1 providing insufficient current share
D4	PS4 providing insufficient current share
D5	PS5 providing insufficient current share
D6	PS6 providing insufficient current share
D7	PS7 providing insufficient current share
D8	PS8 providing insufficient current share
F0	Exhaust Fan 0 failure
F1	Exhaust Fan 1 failure
F2	Exhaust Fan 2 failure
F3	Exhaust Fan 3 failure
F4	Exhaust Fan 4 failure
F5	Exhaust Fan 5 failure
F6	Exhaust Fan 6 failure
F7	Exhaust Fan 7 failure
F8	Door Fan 1 failure
F9	Door Fan 2 failure

Field Support Tech Tip

Product: C-24x
Tech Tip Number: CPU-020
Date: October 31, 1990
Subject: C2xxw ESM & ESMI Codes
Submitted By: Al Haddix

ESM Error and Message Codes

Code	Error/ Message
00	Deadman timer indicates scm internal problem
02	SP-SM.PWRINTAK* failure
04	SP-SM.smbdata<7..0>* failure
07	SP-SM.SPUDCOK failure
08	A/D Converter Timed out
0B	SP2/SP4 invalid command code
0D	SP4 Instruction cycle timed out
0E	Inter-chassis cable incorrect
0F	Checksum failure on ESM
10	VPDA installed incorrectly
11	VPCA installed incorrectly
12	EDCA installed incorrectly
13	EFUA installed incorrectly
14	IPPA installed incorrectly
15	ASPA installed incorrectly
16	VPDB installed incorrectly
17	VPCB installed incorrectly
18	EDCB installed incorrectly
19	EFUB installed incorrectly
1A	IPPB installed incorrectly
1B	ASPB installed incorrectly
1C	SP4 installed incorrectly
1D	CUE installed incorrectly
1E	ME0 installed incorrectly
1F	MO0 installed incorrectly
20	ME1 installed incorrectly
21	MO1 installed incorrectly
22	ME2 installed incorrectly
23	MO2 installed incorrectly
24	ME3 installed incorrectly
25	MO3 installed incorrectly
26	CU0 installed incorrectly
27	ASPC installed incorrectly
28	IPPC installed incorrectly
29	EFUC installed incorrectly
2A	EDCC installed incorrectly
2B	VPCC installed incorrectly
2C	VPDC installed incorrectly
2D	ASPD installed incorrectly
2E	IPPD installed incorrectly

ESM Error and Message Codes (cont)	
Code	Error/ Message
2F	EFUD installed incorrectly
30	EDCD installed incorrectly
31	VPCD installed incorrectly
32	VPDD installed incorrectly
33	PIX installed incorrectly
34	PIY installed incorrectly
35	CXMA installed incorrectly
36	CXMB installed incorrectly
37	CXMC installed incorrectly
38	CXMD installed incorrectly
39	PIV installed incorrectly
3A	PIW installed incorrectly
61	Left PS1 AC power failure
62	Left PS2 AC power failure
64	Left PS4 AC power failure
65	Left PS5 AC power failure
66	Left PS6 AC power failure
67	Left PS7 AC power failure
68	Left PS8 AC power failure
69	Left +5V DC power supply failure
6A	Left +12V DC power supply failure
6B	Left -12V DC power supply failure
6C	Left -5V DC power supply failure
6D	Left -4.5V DC power supply failure
6E	Left -2V DC power supply failure
71	Right PS1 AC power failure
72	Right PS2 AC power failure
75	Right PS5 AC power failure
76	Right PS6 AC power failure
77	Right PS7 AC power failure
79	Right +5V DC power supply failure
7A	Right +12V DC power supply failure
7B	Right -12V DC power supply failure
7C	Right -5V DC power supply failure
7D	Right -4.5V DC power supply failure
7E	Right -2V DC power supply failure
81	Left PS1 current share failure
84	Left PS4 current share failure
85	Left PS5 current share failure
86	Left PS6 current share failure
87	Left PS7 current share failure
88	Left PS8 current share failure
89	Left -4.5V current share out of tolerance
8A	Left -2V current share out of tolerance

ESM Error and Message Codes (cont)

Code	Error/ Message
95	Right PS5 current share failure
96	Right PS6 current share failure
97	Right PS7 current share failure
99	Right -4.5V current share out of tolerance
A0	Left intake thermistor exceeds tolerance
A1	Left exhaust thermistor exceeds tolerance
A2	Left under carriage airflow failure
A4	CUE airflow failure
A5	CUO airflow failure
A9	Left +5V power exceeds tolerance
AD	Left -4.5V power exceeds tolerance
AE	Left -2V power exceeds tolerance
B0	Right intake thermistor exceeds tolerance
B1	Right exhaust thermistor exceeds tolerance
B2	Right under carriage airflow failure
B5	PIY airflow failure
B6	SCM thermistor exceeds tolerance
B9	Right +5V power exceeds tolerance
BA	Right +12V power exceeds tolerance
BB	Right -12V power exceeds tolerance
BC	Right -5V power exceeds tolerance
BD	Right -4.5V power exceeds tolerance
BE	Right -2V power exceeds tolerance
C0	Insufficient power supplies for board configuration
E0	Left FN0 failure
E1	Left FN1 failure
E2	Left FN2 failure
E3	Left FN3 failure
E4	Left FN4 failure
E5	Left FN5 failure
E6	Left FN6 failure
E7	Left FN7 failure
EA	Left power supply fan failure
F0	Right FN0 failure
F1	Right FN1 failure
F2	Right FN2 failure
F3	Right FN3 failure
F4	Right FN4 failure
F5	Right FN5 failure
F6	Right FN6 failure
F7	Right FN7 failure
FA	Right power supply fan failure

Field Support Tech Tip

Product: C1/C2
Tech Tip Number: CPU-021
Date: 03/27/90
Subject: PETS
Submitted By: Brenner/Haddix

Introduction

PETS has now been released PETS to the field for general use.
For those of you who don't know, PETS is a version of the RP scripts which systems test has been running to qualify systems before shipment.

PETS has undergone a reasonably diverse beta test and in that process has been loaded on 14 systems in the field. All problems found during this test period has resulted in changes to the PETS software, so that now it is far easier to load and run.
If you do have problems in running PETS, please contact the TAC.

PETS will be most useful in qualifying newly installed systems, as the previous method of just running diagnostics has proved inadequate in locating suspect components during installation. In addition PETS can be useful in making highly intermittent problems occur in a reasonably short period, thus making repairs far quicker and easier to accomplish. This should result in a higher customer satisfaction. PETS can also be used to help verify customer application problems and determine if they might be a software or hardware bug.

PETS is a suite of application programs that have proved helpful in locating OS and hardware bugs in the past. It's primary purpose is to enhance possible failure modes and increase confidence in newly installed systems.

In addition to PETS, a troubleshooting flow chart is being released.
The part number of this document is 317-000100-01.
This flow chart was a joint effort by product engineering, systems test and the TAC and we hope a very straight forward and smooth approach to repairing various C2 failures. These flow charts can be used in standard crashes and hangs and also includes coverage of troubleshooting by the use of PETS. We hope that this is of use to the field. Eventually it should be incorporated into the CONVEX troubleshooting guide that is included with the C2 maintenance documentation.

PETS uses and limitations

Now that PETS has arrived in the field, it is important to discuss the limitations and intended use of PETS.

First let me explain that PETS is not a cure all, nor is it intended to be the sole diagnostic procedure that we are to use. This is especially true of installations.

PETS is an excellent tool, when run with diagnostics, to qualify a new system. It is also a tool to use on stubborn intermittent failures that could take weeks to solve otherwise. These are considered the situations where PETS "MAY" be of use.

PETS is not considered a diagnostic tool in itself. PETS does not run parallel code and it is a poor I/O exerciser. PETS is really only a head and memory exerciser.

It is entirely possible to have a hardware problem and for PETS to run flawlessly. It has even been observed that the error can be hard enough as to fail diagnostics and still run PETS successfully.

PETS is only considered a diagnostic tool to be used when other tools prove inadequate. As mentioned earlier, it is also to be run at installation in conjunction with the field diagnostic scripts.

Hints on Installing and Running PETS

--Make backup copies of any system files before you modify them.--

1. Login as root.

2. Locate a disk partition with at least 100 meg of available space. Block size cannot be larger than 8k/2k on the disk partition to which PETS is loaded. Tests will core dump if it is.

3. Mount PETS tape and use "/etc/installsw -i" to install PETS. If the install directory is not "/mnt" type full pathname when asked.

4. Edit "/etc/rc.local" so batch ques and shares(nqs daemon) won't start at reboot time. You might also want to prevent the network daemons from starting.

5. Remove any aliases in the ".cshrc" file.

6. Edit root's ".login". Add "." to the setpath line if it is not there. Remove any aliases in the ".login" file.

7. Reboot system to "spu >".

8. If there is a "/mnt/os/bootcmd.local", "mv" it to a backup file.

9. Edit "/mnt/os/bootcmd", add "tune cpu maxusers = 256" to this file.

10. Boot to "multi-user".

11. Login as root. "touch" /etc/nologin, to keep users off the system.

12. "cd" to PETS directory. Execute "run", "run24", "run48" or "run96" according to the directions in the PETS "README" file.

13. It is NOT advisable to run the "systems" or "screener" scripts in the field. These scripts may cause FALSE crashes in the field.

14. Monitor PETS with the "status" program.

15. If any errors are encountered, refer to the Troubleshooting Flowcharts (doc.#317-000100-001)for troubleshooting hints.

16. When PETS run is complete, the "status" program will display a "Completed" message and then restart.

17. To terminate the PETS program use the "jobs" command to find the job #'s and then use the "kill ?%" (?= job # to be killed).

18. When finished running PETS, be sure to return any modified system files to their original condition, then reboot.

19. You should remove the PETS directory with the "rm -r" command before giving the system back to the customer.

Troubleshooting with PETS

Always check the error file when there is a failure using PETS. The following is an example of what happens when PETS tries to use the memory and swap space of a system beyond the systems configured physical limitations. This occurred on a C-240 with 256 Mbyte of memory and two one gig disk drives using the 'b' partition of each drive for swap space.

The failure below IS NOT due to a hardware problem.

```
Head: B
PROCESS NAME____# PASSES MEMORY UNLIMITED____# PASSES MEMORY LIMITED TO 4KBYTES
 test.019_1_1 test.015__4__4 test.002__24__24 test.006_125_125 test.012_125_125
 test.020_1_1 test.004__5__5 test.003__24__24 test.008_125_125 test.227_125_125
 test.023_1_1 test.001__7__7 test.022__84__84 test.009_125_125
 test.999_1_1 test.024__7__7 test.026_124_124 test.010_125_125
 test.014_4_4 test.007_12_12 test.005_125_125 test.011_125_125
No match.
Processes/test.026/LIMIT_B_1/test.026.COREDUMP.Jan27.13:38:56
5:05pm  up  5:49,  2 users,  load average: 116.69, 115.42, 115.09
```

By changing to PETS/Processes/test.026/LIMIT_B_1 and examining file test.026.COREDUMP.Jan27.13:38:56 it is easy to determine that the error is not an actual hardware failure. The contents of this file can be found below.

../../../bin/mpa: execve of <../test.026> failed Insufficient free swap space

It is important to remember that not all errors received by PETS are hardware failures and because of this all errors should be examined before attempting any hardware solutions.

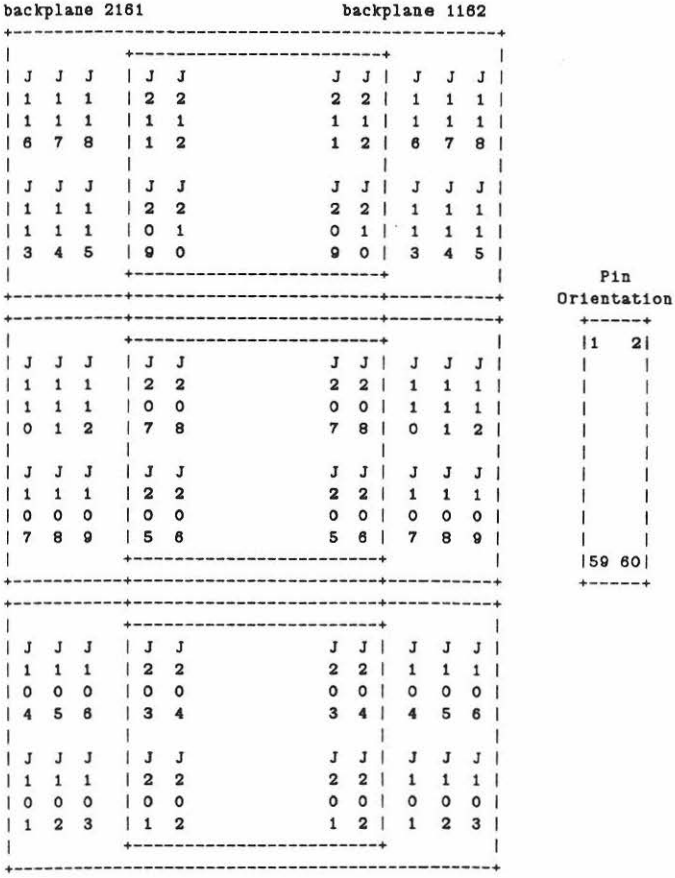
CONVEX

Field Support Tech Tip

Product: C240
Tech Tip Number: CPU-022
Date: 03/15/90
Subject: C240 Flex Circuit Identification
Submitted By: Brenner

C240 Flex Circuit Identification

The following is the connector identification for the flex circuits which interconnect the 2161 and 1162 backplanes. As viewed from the rear of the cabinets bolted together. Use extreme care during installation and removal of the flex connector circuits.



CONVEX

Field Support Tech Tip

Product: C2 Widebody
Tech Tip Number: CPU-023
Date: 03/27/90
Subject: Memory Backplane SIP Locations
Submitted By: Brenner

500-001162-200

Memory backplane SIP locations viewed from rear of machine.

	P2-CUO			P2-ME3			P2-M03			P2-CUE			P2-SP4
SP6		LB8	LB20	LB902	LC10	LC1411	LC903	RA31	RA1159	RA35		LA87	LA906	
RB906		LB79		LB115	LC15	LC57	LC902	RA47	RA1136	RA901		LA78	LA905	LA901
RB1665		LB1669	LB135	LB150	LC9901	LC30	LC174	RA69	RA1130	RA122		LA9903	LA904	LA914
RB907		LB1666	LB132	LB147	LC38	LC62	LC22	RA1661	RA9902	RA903		LA1667	LA1339	LA913
RB93		LB9901	LB67	LB143	LC50	LC71	LC12	RA1555	RA1113	RA1229		LA108	LA910	LA912
RB905		LB1600	LB127	LB65	LC6	LC73	LC1106	RA45	RA1101	RA1125		LA99	LA9099	LA911
RB173		LB1588	LB555	LB16	LC34	LC266	LC94	RA17	RA922	RA1118		LA882	LA1022	LA9022
RB134		LB28		LB54	LC19	LC48	LC72	RA157	RA86	RA1172		LA91	LA75	LA9115

500-001162-200

Memory backplane SIP locations viewed from rear of machine (continued).

	P1-CU0			P1-ME3			P1-MO3			P1-CUE			P1-SP4
SP5		LB98	LB164	LB25	LC11	LC334	LC124	RA43	RA600	RA449	LA1170	LA174	LA908	
		LB96	LB85	LB119	LC88	LC7	LC21	RA1096	RA666	RA37	LA1682	LA1444		
RB128		LB76	LB154	LB51	LC688	LC27	LC63	RA1533	RA1711	RA145	LA444	LA1377	LA168	
RB120		LB61	LB152	LB83	LC24	LC18	LC32	RA81	RA644	RA1400	LA11177	LA1331	LA1448	
RB112		LB42	LB1	LB3	LC39	LC176	LC36	RA13	RA70	RA2	LA144	LA1221	LA151	
RB103		LB29	LB97	LB1168	LC58	LC400	LC59	RA9	RA588	RA1468	LA1004	LA11144	LA133	
RB142		LB23	LB105	LB53		LC52	LC41	RA1388	RA1633	RA1110	LA90	LA1044	LA1111	
		LB107	LB1586	LB89	LC5		LC466	SP7				SP4		

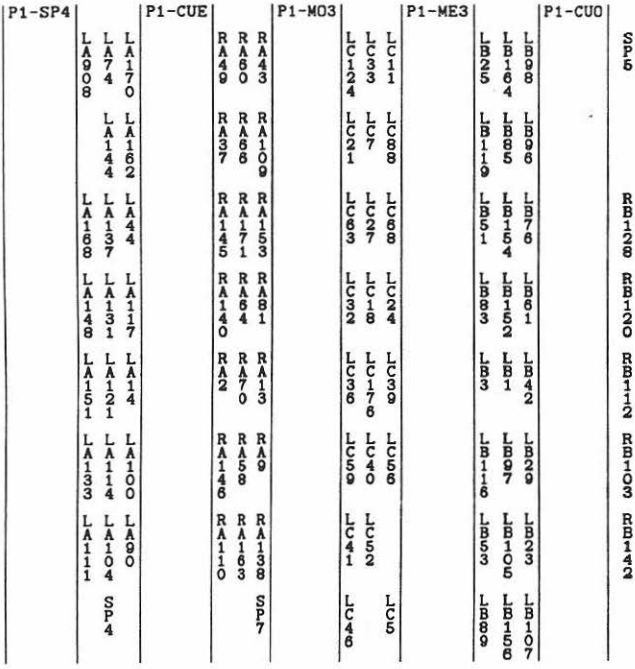
500-001162-200

Memory backplane SIP locations viewed from the front looking into the chassis.

P2-SP4			P2-CUE			P2-MO3			P2-ME3			P2-CUO	
	LA906	LA87		RA35	RA159	RA31	LC903	LC141	LC10	LB902	LB20	LB8	SP6
LA901	LA905	LA78		RA901	RA136	RA47	LC902	LC57	LC15	LB115		LB79	RB906
LA914	LA904	LA903		RA122	RA130	RA69	LC174	LC30	LC901	LB150	LB135	LB169	RB165
LA913	LA139	LA167		RA903	RA902	RA161	LC22	LC62	LC38	LB147	LB132	LB166	RB907
LA912	LA910	LA108		RA129	RA113	RA155	LC12	LC71	LC50	LB143	LB67	LB901	RB903
LA911	LA909	LA99		RA125	RA101	RA45	LC106	LC73	LC6	LB65	LB127	LB160	RB905
LA902	LA102	LA82		RA118	RA92	RA17	LC94	LC26	LC34	LB16	LB55	LB158	RB173
LA915	LA75	LA91		RA172	RA86	RA157	LC72	LC48	LC19	LB54		LB28	RB134

500-001162-200

Memory backplane SIP locations viewed from the front looking into the chassis (continued).



Spare pin locations for the 1162 backplane. Verify a location has not been used by a later ECN or flaw rework before using that location.

1162 backplane location	100 ohm terminators sip size	* SPARE PINS
LA108	TM9100	* 6, 7.
LA117	TM9100	* 1, 9.
LA14	TM9100	* 4, 6, 7, 9.
LA162	TM9100	* 3.
LA167	TM9100	* 1, 6.
LA170	TM9100	* 1, 3.
LA74	TM9100	* 1, 3, 6.
LA82	TM9100	* 4.
LA90	TM9100	* 1, 3, 7, 9.
LA901	TM9100	* 1, 3, 4, 6, 7.
LA902	TM9100	* 1, 3, 4, 6, 7.
LA904	TM9100	* 9.
LA905	TM9100	* 1, 3.
LA906	TM9100	* 1.
LB1	TM9100	* 7, 9.
LB152	TM9100	* 1.
LB156	TM9100	* 1, 3, 7, 9.
LB158	TM9100	* 4.
LB164	TM9100	* 1.
LB28	TM9100	* 6, 7, 9.
LB79	TM9100	* 3.
LC10	TM9100	* 1.
LC11	TM9100	* 1, 3, 4, 6.
LC15	TM9100	* 1, 3.
LC174	TM9100	* 9.
LC176	TM9100	* 7, 9.
LC18	TM9100	* 1, 3.
LC19	TM9100	* 6, 7, 9.
LC24	TM9100	* 1, 3, 4, 7, 9.
LC33	TM9100	* 1, 3.
LC34	TM9100	* 4.
LC39	TM9100	* 4, 6, 7, 9.
LC5	TM9100	* 1, 3, 4, 9.
LC50	TM9100	* 6.
LC56	TM9100	* 1, 3, 4, 6.
LC68	TM9100	* 3, 4, 9.

LC7	TM9100	* 3, 4, 6.
LC88	TM9100	* 1, 3, 4.
LC901	TM9100	* 4, 6, 7, 9.
RA153	TM9100	* 3.
RA155	TM9100	* 6.
RA157	TM9100	* 9.
RA171	TM9100	* 9.
RA2	TM9100	* 7, 9.
RA43	TM9100	* 1, 3.
RA81	TM9100	* 1.
RA9	TM9100	* 1.
RA901	TM9100	* 3.
RA902	TM9100	* 1, 3.

1162 backplane 50 ohm terminators

location	sip size	* SPARE PINS
LA104	TM9050	* 4, 6, 7, 9.
LA111	TM9050	* 3, 4, 6, 7, 9.
LA144	TM9050	* 7.
LA75	TM9050	* 3, 6, 7, 9.
LA87	TM9050	* 1, 3, 4.
LA908	TM9050	* 1, 3, 4, 6, 7.
LA91	TM9050	* 9.
LA911	TM9050	* 1, 3.
LA912	TM9050	* 9.
LA913	TM9050	* 4, 6.
LA915	TM9050	* 3, 4, 6, 7, 9.
LB105	TM9050	* 4, 6, 7, 9.
LB107	TM9050	* 4, 6, 7, 9.
LB115	TM9050	* 4.
LB127	TM9050	* 1, 3, 4, 6, 9.
LB132	TM9050	* 3, 4, 6, 7.
LB135	TM9050	* 1, 4, 7.
LB143	TM9050	* 7.
LB147	TM9050	* 7.
LB20	TM9050	* 1, 3, 4, 6, 7.
LB23	TM9050	* 3, 4, 6, 7, 9.
LB25	TM9050	* 1, 3.
LB54	TM9050	* 4, 9.
LB55	TM9050	* 6, 7, 9.
LB65	TM9050	* 9.

LB67	TM9050	* 3, 4, 7, 9.
LB76	TM9050	* 1.
LB85	TM9050	* 7.
LB89	TM9050	* 6, 7, 9.
LB902	TM9050	* 1, 3, 7.
LB96	TM9050	* 1, 3, 4, 6, 7.
LB98	TM9050	* 1, 3, 4.
LC106	TM9050	* 1, 3, 4.
LC12	TM9050	* 9.
LC141	TM9050	* 1.
LC22	TM9050	* 4, 6, 7.
LC26	TM9050	* 7.
LC41	TM9050	* 9.
LC46	TM9050	* 4, 6, 7, 9.
LC48	TM9050	* 9.
LC52	TM9050	* 7, 9.
LC62	TM9050	* 4.
LC72	TM9050	* 1, 6, 9.
LC73	TM9050	* 4.
LC902	TM9050	* 6.
LC903	TM9050	* 1.
LC94	TM9050	* 6, 7, 9.
RA110	TM9050	* 9.
RA163	TM9050	* 9.
RA49	TM9050	* 1.
RB112	TM9050	* 1, 3, 4, 6.
RB128	TM9050	* 1.
RB142	TM9050	* 4, 6, 7, 9.
RB165	TM9050	* 6, 7.
RB173	TM9050	* 1.
RB906	TM9050	* 1.
RB93	TM9050	* 3,4,6.

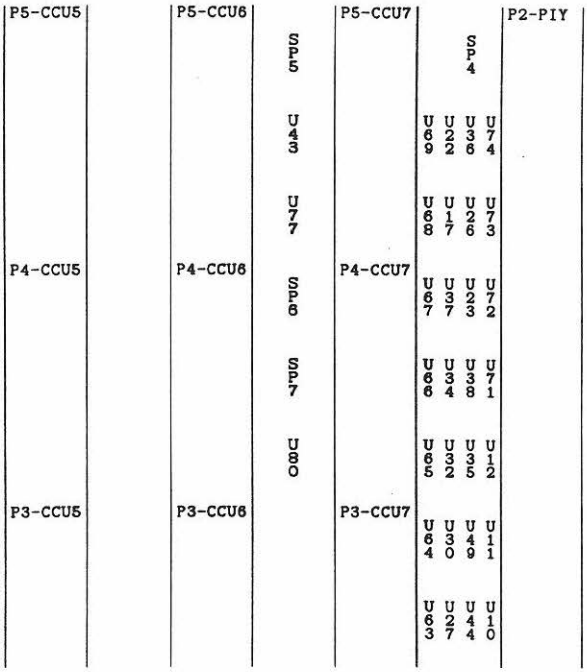
CONVEX

Field Support Tech Tip

Product: C2 Widebody
Tech Tip Number: CPU-024
Date: 03/28/90
Subject: I/O Backplane SIP Locations
Submitted By: Brenner

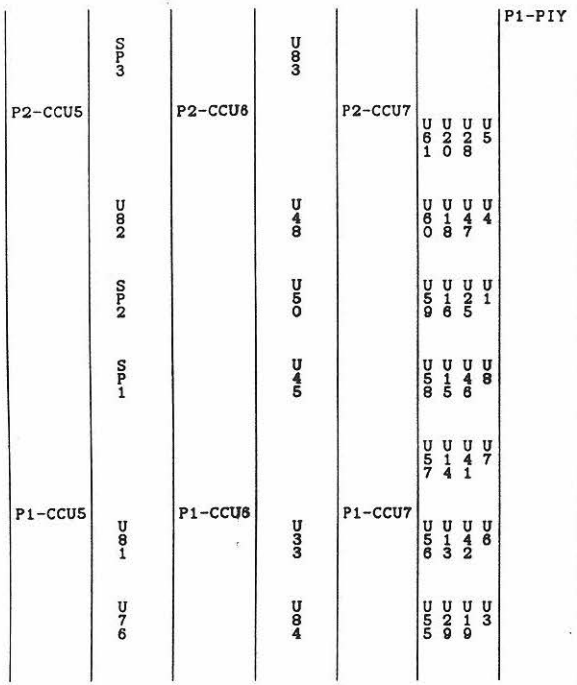
500-002161-200

I/O backplane SIP locations viewed from rear of machine.



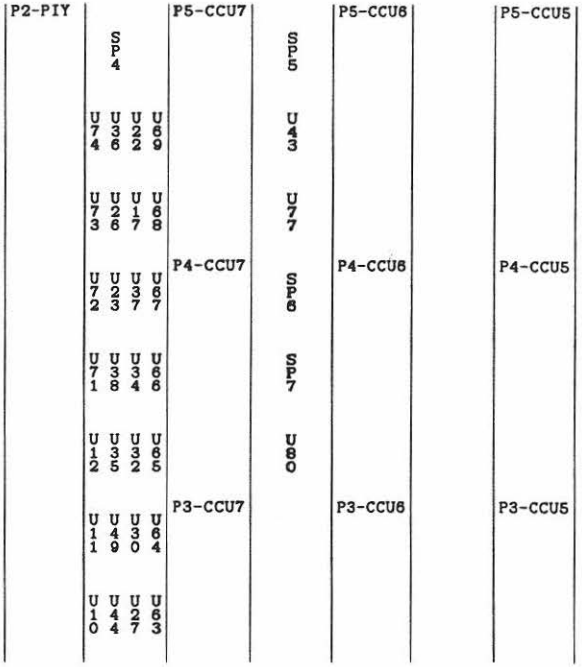
500-002161-200

I/O backplane SIP locations viewed from rear of machine (continued).



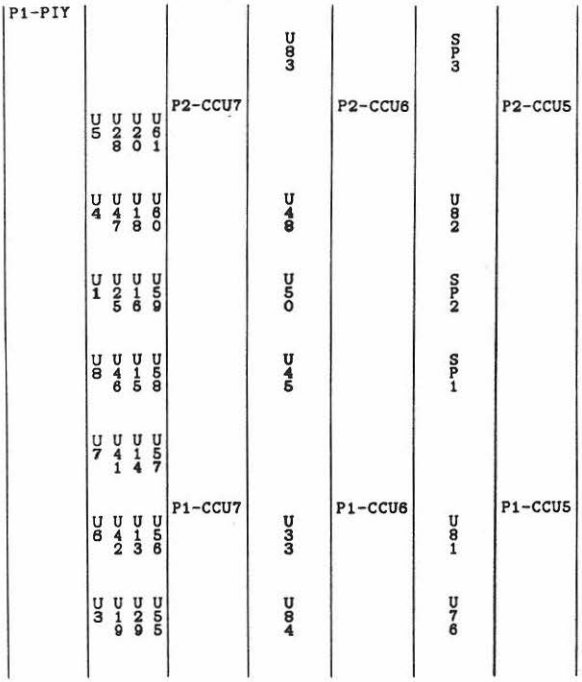
500-002161-200

I/O backplane SIP locations viewed from the front looking into the chassis.



500-002161-200

I/O backplane SIP locations viewed from the front looking into the chassis (continued).



Spare pin locations for the 2161 backplane. Verify a location has not been used by a later ECN or flaw rework before using that location.

2161 backplane location	100 ohm terminators sip size	* SPARE PINS
U73	TM9100	* 4.
U72	TM9100	* 4.
U71	TM9100	* 1.
U68	TM9100	* 4, 6.
U67	TM9100	* 4, 6, 7.
U66	TM9100	* 1, 3.
U65	TM9100	* 3, 6, 7, 9.
U64	TM9100	* 1, 3, 7, 9.
U63	TM9100	* 3, 4, 7, 9.
U60	TM9100	* 1, 3, 6, 7.
U58	TM9100	* 4, 6.
U57	TM9100	* 6, 7.
U55	TM9100	* 3, 4, 6, 7, 9.
U49	TM9100	* 9.
U47	TM9100	* 1, 7.
U46	TM9100	* 6.
U44	TM9100	* 9.
U41	TM9100	* 7.
U38	TM9100	* 1.
U37	TM9100	* 4.
U35	TM9100	* 7, 9.
U34	TM9100	* 1.
U32	TM9100	* 3, 7, 9.
U30	TM9100	* 7, 9.
U29	TM9100	* 4, 6, 7, 9.
U27	TM9100	* 4, 9.
U26	TM9100	* 4.
U23	TM9100	* 4.
U19	TM9100	* 4 , 6, 7, 9.
U18	TM9100	* 1, 3, 6, 7.
U17	TM9100	* 4, 6.
U15	TM9100	* 6.
U14	TM9100	* 7.
U12	TM9100	* 7, 9.
U10	TM9100	* 7, 9.
U4	TM9100	* 1.
U3	TM9100	* 4.

2161 backplane 50 ohm terminators

location	sip size	* SPARE PINS
U33	TM9050	* 6.
U43	TM9050	* 1, 3, 4.
U48	TM9050	* 7.
U50	TM9050	* 1, 3, 4, 6, 7.
U76	TM9050	* 7, 9.
U77	TM9050	* 1, 3, 9.
U80	TM9050	* 1, 3.
U81	TM9050	* 1, 3, 4, 6, 7.
U82	TM9050	* 7, 9.
U83	TM9050	* 1, 3, 4, 6, 7.
U84	TM9050	* 9.

Field Support Tech Tip

Product: C-2
Tech Tip Number: CPU-025
Date: May 25, 1990
Subject: Something New
Submitted By: Al Haddix

NEW CRASHDUMP SWITCH

The utility crashdump has been modified with the 8.0 release of OS. This utility now includes a new switch (-H) which includes a hardware dump with the standard crashdump. This will all be dumped to tape. The hardware dump taken for the crashdump can not be used in place of a standard hwdump as it will not create this file on the spu disk, only on tape.

It is recommended that the crashdump -H be taken for any crash or hang where software is suspected. It will be necessary to acquaint your customers with this method of taking a crashdump. The proper procedure for securing a crashdump follows:

1) osclean (stops all processes running, if a hang)
2) crashdump -H

In cases where software is not suspected, or on initial crashes, it is recommended that the standard hwdump procedure be followed, as the vast majority of all crashes and hangs are hardware related. If a crashdump is necessary, it is recommended that it be taken prior to running any other utility before accomplishing this crashdump. After the crashdump is complete then other troubleshooting can proceed.

PETS OPERATIONAL NOTES

It has recently been discovered that an OS bug exists in all releases of CONVEX OS that affects the operation of PETS.

This bug can cause an unexpected crash when any process that examines the proc table is run concurrently with PETS. This bug will only happen under very specific circumstances and so is not seen often. The specific error witnessed is a "Fatal Convex Unix Error (Unresolved kernel PTE violation)". It is also felt that other crashes can result from this interaction. Because of this, any crash suffered during the execution of PETS and one of these processes, that has not been seen on the system before, be viewed with suspicion.

The processes that examine the proc table are as follow:

1) ps
2) syspic
3) w
4) sysex

If a crash should occur, be very suspicious of any crash that has not been experienced on this system previously. This can save many wasted hours of troubleshooting in the wrong direction.

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REDUCED HWDUMP

I would like to recommend that the vp_scn and icache portion of the hwdump be disabled from the hwdump utility. This can be done because less than 1% of system crashes or hangs actually require this information. On the benefit side, it will allow hwdump to complete in less than 1/3 of the time and means that when faxing information it is not necessary to delete the icache and vp_scn info to make it faxable. It also means that when saving these dumps on the spu, the dump will take up much less disk space.

To disable these functions, first copy hwdump_iscn to another file. We don't want to delete this because it is possible that the full version will be required for some crash in the future. The following module will exist for each head at the end of the file **/hw/cputest/hw_iscn**:

```
:13 = bt asp[3]: "asp"
if (:13 == 0) then {
        :900=3
     dump_head()
     !echo "CPU D Icache" >> XxX.3
     !icache -c 3 >> XxX.3
     !echo "CPU D Vector Registers" >> XxX.4
     !vp_scn < hwdump_vpscn_d >> XxX.4
} else { pr "Oo CPU D Present0 }
# Quit
```

As can be seen from the example, it is a simple matter to delete the entries for icache and vp_scn. A like module exists for each head and must be deleted for each head. Please leave in the entries for the echo so that the fact that this hwdump has been modified can be readily identified.

Again, this can be quite a time saver and is recommended when possible.

CONVEX

Field Support Tech Tip

Product: C-2
Tech Tip Number: CPU-026
Date: May 25, 1990
Subject: ATTENTION Light
Submitted By: Kelvyn Gipp

A problem has been found on a Rev. Z 130 SCM, and a Rev J 168 SCM that affects the operation of the system ATTENTION light.

With the above revisions, when the system detects an error that turns on the ATTENTION light, **the ONLY way this can be cleared is for the system to be powered down and the system main circuit breaker to be turned off.**

Turning the key-switch off, or using the "sp2util" procedure **WILL NOT** accomplish this. This problem will be corrected in the Rev K 168, and the Rev AA on the 130 SCM's.

With other Revisions of SCM, it is possible to reset the ATTENTION light by utilizing the following procedure:

TURNING OFF THE C2 ATTENTION LIGHT

1. Commands typed in at the system console:

System PROMPT	Your INPUT	Explanation
#	^p	(go to the SPU prompt, or skip this step if you are already at the SPU prompt.)
(spu)>	sp2util	(start the sp2util utility)
sp2util:	rm cpr	(display cpr register contents)
<cpr(ffd029> = ab	nx	(where the 'a' in the value displayed equals the 'n', and the value "x" is the 'b' value less the ERROR bit. (SEE NOTE FOLLOWING PAGE)
<trr(ffd???> = ??	q	(q for quit, no further locations require changing)
sp2util:	q	(q for quit, exit the sp2util utility)
(spu)>	^d	(go to multi-user)
#		

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2. The commands used on the previous page change the rightmost four bits of a register. These four bits refer to the following flags:

ERROR	RUN	LOCAL	REMOTE

NOTE

The initial value retrieved for the hex value (x) can differ depending upon the state of the system. As an example, assume the system was RUNning, in LOCAL, and the ERROR bit was set, the retrieved value would be "nE". See Example 1 below.

EXAMPLE 1

ERROR	RUN	LOCAL	REMOTE
1	1	1	0

When this value is changed to a "n6", you are turning off the ERROR bit, and thus the Attention light. See Example 2 below.

EXAMPLE 2

ERROR	RUN	LOCAL	REMOTE
0	1	1	0

CONVEX

Field Support Tech Tip

Product: C-2
Tech Tip Number: CPU-027
Date: July 27, 1990
Subject: Environmental Errors
Submitted By: Al Haddix

It is important to understand that the C2 no longer has a problem with errorneous environmental errors. Previously because the SCM's were overly sensitive to noise and would produce environmental error like the example:

EXAMPLE

```
% [SPU  @12:05:36] errintd:   enviornmental error
[SPU  @12:05:36]    EMR indicates no problems -
[SPU  @12:05:37]    power supplies, fans, and temperature sensors will be
                    checked
[SPU  @12:05:37]    SCM temp: 25 deg C (0x80) is not greater than 56 deg C
                    (0x3a)
[SPU  @12:05:37]    intake temp: 21 deg C (0x8c) is not greater than 38 deg C
                    (0x5d)
[SPU  @12:05:37]    exhaust temp: 34 deg C (0x68) is not greater than 56 deg C
                    (0x3a)
[SPU  @12:05:37]    all fans ok
[SPU  @12:05:37]    +5: n  +5.13 VDC (0xec) within +4.87 (0xe0) and +5.18
                    (0xee)
[SPU  @12:05:38]    +12: n +12.07 VDC (0xba) within +11.42 (0xb0) and +12.59
                    (0xc2)
[SPU  @12:05:41]    -5: n  -5.09 VDC (0xea)  within -5.33 (0xf5) and -4.80
                    (0xdd)
[SPU  @12:05:41]    -12: n -12.00 VDC (0xb9)  within -12.59 (0xc2) and -11.42
                    (0xb0)
[SPU  @12:05:41]    -2: n  -2.02 VDC (0xcf)  within -2.10 (0xd7) and -1.96
                    (0xc9)
[SPU  @12:05:41]    -4.5: n  -4.52 VDC (0xe7)  within -4.68 (0xef) and -4.40
                    (0xe1)
[SPU  @12:05:44]    UNABLE TO DETERMINE CAUSE OF ENVIORNMENTAL ERROR
[SPU  @12:05:44]    CHECK SM BOARD AND FIRMWARE REVISIONS FIRST
```

This error basically indicated that something had occurred, but was of extremely short duration and nothing could be determined to be in error. This problem was corrected in rev X of the 130 SCM, rev G of the 168 SCM and rev N of the ESM. This made the firmware less sensitive and thus prevented the false environmental errors that we had been disabling.

Under the previous circumstances, it was frequently necessary to disable the environmental errors to prevent these errors. That is no longer necessary.

If a C2 experiences these errors now it is not an erroneous error and should not be disabled. This error now indicates that something is wrong, but the SCM/ESM has not been able to locate the problem.

This problem has many times, recently, been determined to be the +5 VDC power supply. By monitoring the error printouts it usually an easy task to spot the power supply that is fluctuating and causing the disturbance. This would indicate a power supply that has become unstable, but in a pinch the +5 VDC supply can be adjusted to 5.05 VDC from the standard 5.1 VDC and this will generally solve the problem, at least until a more permanent solution can be accomplished.

Although it is possible that other problems may generate this error, because the other supplies are shared, this has not occurred yet. But it is a simple matter to find the source by carefully analyzing the previous error printouts.

Again, the above error on a C2 should no longer be disabled, but indicates a true environmental problem on the C2.

Field Support Tech Tip

Product: C-1
Tech Tip Number: CPU-028
Date: August 30, 1990
Subject: CONVEXOS 9.0
Submitted By: Jerry Throgmorton

This Tech Tip describes the various possibilities available when upgrading the ConvexOS to 9.0 on C-1 series computers.

NOTE: When released, the installation of System Diagnostics V6.6 will perform the following procedures semi-automatically.

CONVEXOS 9.0 and IOP/VIOP's

This procedure applies **ONLY** to a C-1 system having **BOTH** IOP's and VIOP's installed.

1) Make a backup of the spu disk.

2) Remove the directory jptest from /mnt.

3) Remove all dev 4xxx and dev 5xxx diagnostics from /mnt/test not needed to troubleshoot that particular system.

4) Load ConvexOS 9.0.

CONVEXOS 9.0 and IOP's

This procedure applies **ONLY** to a C-1 system having **IOP's** with **NO** installed VIOP's.

1) Make a backup of the spu disk.

2) Remove the directory jptest from /mnt.

3) Remove all io/dev 5xxx diagnostics from /mnt/test.

4) Load ConvexOS 9.0.

Steps 2) and 3) will provide 2.6MB of free space. Additional space can be provided by removing all dev 4xxx diagnostics not needed to troubleshoot equipment on the individual system.

This completes the procedure for installing ConvexOS 9.0 on a C-1 that has **ONLY** IOP's installed.

CONVEXOS 9.0 and VIOP's

This procedure applies **ONLY** to a C-1 system having **VIOP**'s with **NO** installed IOP's.

1) Make a backup of the spu disk.

2) Remove the directory jptest from mnt.

3) Remove all io/dev 4xxx diagnostics from /mnt/test.

4) Load ConvexOS 9.0.

Steps 2) and 3) will provide 3.8MB of free space. Additional space can be provided by removing all dev 5xxx diagnostics not needed to troubleshoot equipment on the particular system.

This completes the procedure for installing ConvexOS 9.0 on a C-1 that has **ONLY** VIOP's installed.

CONVEX

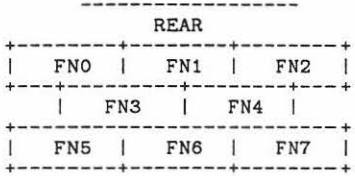
Field Support Tech Tip

Product: C2XX
Tech Tip Number: CPU-029
Date: October 31, 1990
Subject: Fan Locations
Submitted By: Kelvyn Gipp

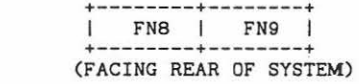
The following information is provided as a quick reference chart.

SIX FAN ASSEMBLY

EIGHT FAN ASSEMBLY



TWO FAN ASSEMBLY



SINGLE FAN ASSEMBLIES

Single fan assemblies reside in each of the wide-body cabinets. Each fan assembly is located in the left-hand side of the bottom of each cabinet, when viewed from the front.
If an error occurs in either of these fan assemblies:

The Left Cabinet fan will produce an **"EA"** ESM error code.

The Right Cabinet fan will produce an **"FA"** ESM error code.

EXP-105 CABINET FANS